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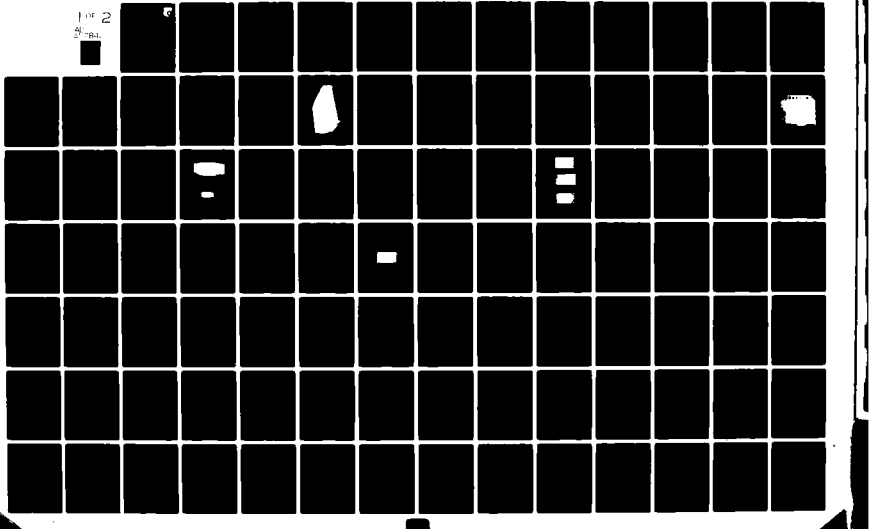

AFWAL-TR-81-4038

# ADVANCED NONDESTRUCTIVE EVALUATION (ULTRASONIC PULSER/RECEIVER TECHNOLOGY)

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Final Report for Period May 29, 1979 through February 1, 1981



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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The overall goal of this program was to develop a digital ultrasonic correlation system for NDE application of greater versatility and capability than the successful analog system developed in-house at AFWAL/MLLP. SRL had only limited success in meeting this overall goal. The program broke into two complementary tasks: (1) development of an all-digital Pulser/Receiver with a bandwidth of 85 MHz and a maximum gain of 80 dB; and (2) development of a pseudo-random correlation unit. The Pulser/Receiver met all of its necessary requirements; however, the correlation unit suffered from a technical design

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decision made early in the program as to the number of "bits" used in the correlation process. The decision (based upon both cost and the results of the computer model of an 8-bit correlation system) was to utilize 1-bit correlation. This choice led to an unavoidable (and most undesirable) nonlinearity in the correlated signal output when the input signal/noise ratio approached unity. This unfortunate consequence has restricted the versatility and capability of the entire system.

In its favor, the system has demonstrated the basic principle of an all-digital approach to pseudo-random signal correlation. Also, the computer model indicated that the possibility exists for compensating for the nonlinearity in the microcomputer. The current hardware system will allow this approach to be further pursued after a more exhaustive laboratory evaluation provides the necessary corrective algorithms.

Met all necessary requirements with the exception of the self-calibration function.

## CITATION

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# SECTION I
# INTRODUCTION

The requirements of nondestructive evaluation (NDE) of the engine and structural components of military aircraft have increased dramatically in recent years as the utilization of existing aircraft has been extended beyond anticipated lifetimes. Concurrently, the performance requirements of military aircraft have pushed designers even closer to the stress limits of conventional materials and necessitated investigations into new material systems and fabrication techniques such as near-net-shape HIP powdered metals, laminated blades, dual-alloy construction, ceramics, composites, and adhesively-bonded structures. With each new material system or fabrication technique or decrease in flaw size, further demands are placed upon current NDE equipment. Presently the NDE equipment which is available off-the-shelf from commercial suppliers does not meet the current inspection requirements of the USAF, and the problems are not decreasing.

The Materials Laboratory, Air Force Wright Aeronautical Laboratories (AFWAL/MLLP), being aware of these needs, has been funding basic research and development in recent years to improve the detection capabilities of the various NDE technologies. Several of these programs have yielded fundamental advancements in the state of the art. This program was directed toward the development of advanced ultrasonic instruments which will employ new technology to increase sensitivity and answer the specific NDE need of the USAF in the detection of fatigue cracks.

## SECTION II

## PROGRAM OBJECTIVES AND APPROACH

The primary objective of this program was to develop an advanced NDE ultrasonic pulser/receiver inspection system for detecting cracks in aircraft structures which will be capable of an improvement in sensitivity of 20 dB over existing conventional ultrasonic equipment.

To meet these objectives, SRL has produced a high performance, conventional ultrasonic pulser/receiver system; and to further improve the signal-to-noise (S/N) ratio, SRL has produced a high speed, digital Pseudorandom-Binary-Signal Correlation System. The systems incorporate the use of a microprocessor controller to further increase system capability by allowing easy computer interface and the added flexibility necessary for future system expansion.

## SECTION III

## ULTRASONIC PULSER/RECEIVER SYSTEM

### 1. SYSTEM DIAGRAM

The block diagram of the complete pulser/receiver system is shown in Figure 1. The central processing unit is the Intel 8085 and the remote interface conforms to the IEEE-488, general purpose, instrumentation-interface standard. As shown in Figure 1, all elements of the unit are under microprocessor control.

### 2. FRONT PANEL CONTROLS AND DISPLAYS

The microprocessor-based pulser/receiver system allows all switches and controls on the front panel or any command on the interface bus to update the current selected value of any function. The program module increases the capabilities of the system by allowing all control functions to be stored and/or retrieved for any presystem programming applications. All displayed values of critical functions are the actual sampled value of the controlled parameters, and any system difficulties appear as an uncal condition or as error codes on the same display.

The pulser/receiver chassis and front panel are shown in Figure 2. All parameter controls are pushbutton rotary switches, and all mode selects are pushbutton illuminated momentary switches. The microprocessor scans the condition of each switch and updates each parameter according to the switch position. The description of each front panel control is described below.

PRF - Selects the transmitter pulse rate: 10 to 9990 Hz. Selects external input when switch setting reads 000 Hz.

Gain - Selects the RF amplifier gain: -39.9 dB to +79.9 dB in 0.1 dB steps. Selects the log amplifier input gain: -35 dB to +15 db in 10 dB steps.

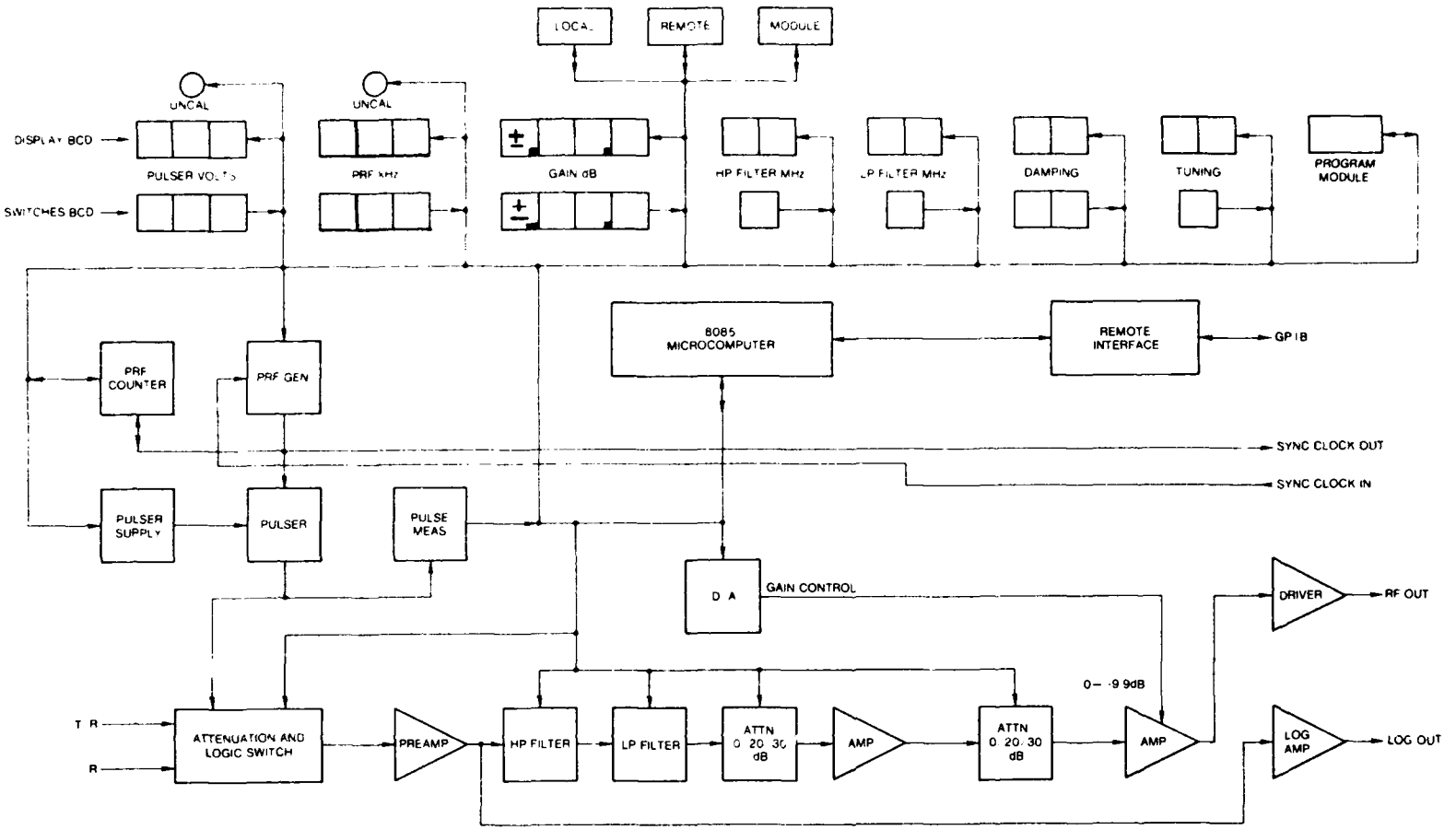


Figure 1. Block Diagram of the Pulser/Receiver System

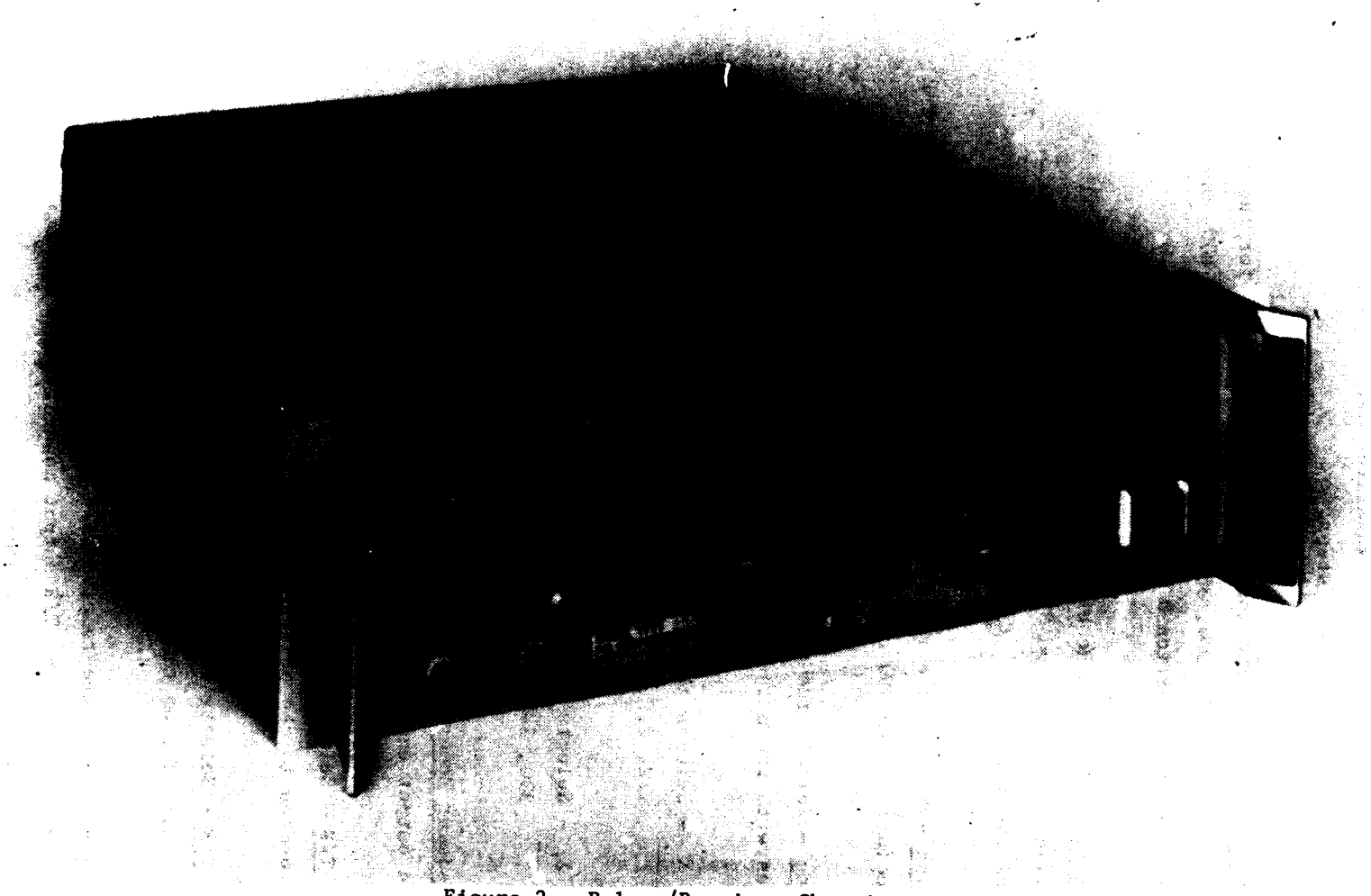

Figure 2. Pulser/Receiver Chassis

Pulser Volts - Selects the transmitter output pulse amplitude: 10 to 990 volts in 10 volt steps.

HP Filter - Selects the low frequency -3 dB point for the RF amplifier: .5, 100, 200, 300, 400, 500, 600, 700, 800, and 900 KHz (switch position 0 through 9, respectively).

LP Filter - Selects the high frequency -3 dB point for the RF amplifier: 10, 25, and 85 MHz (switch position 0 through 2, respectively).

Damping - Selects the resistive impedance at the input to the T/R connector: 10 to 990 ohms in 10 ohm steps.

Tuning - Selects the value of the complex impedance network in series with the output of the transmission pulse.

$X_L$ - Selects the inductive component; .27, .39, .56, .82, 1.2, 2.7, 5.6, 10, or 22 μh.

$X_C$ - Selects the capacitance component; 100, 150, 200, 250, 300, 390, 500, 680, 820, or 1000 pf.

Transducer Mode - Selects the operation mode to the transmission pulse output and the amplifier input.

T/R - Selects transmit and receive mode: amplifier connected to the pulser output.

T>R - Selects the through transmission mode: pulser output isolated from the amplifier input.

R - Selects the receive-only mode. Transmission pulse isolated from the T/R output connector and the amplifier connected to the R connector.

Off - Selects the off mode. The transmission pulse output and amplifier input are isolated from the T/R and R connectors.

Control Mode - Selects the control mode for the instrument.

Local - Selects instrument control via the front panel switches.

Remote - Selects instrument control via the IEEE-488 computer bus interface.

Module - Selects instrument control via the program module.

Program No. - Selects the module program number to control the instrument or to be programmed by the instrument.

Reset - Enters the control data from the module into the instrument program storage memory when operating in the module mode.

Alter - Allows for the control change of any front panel switch setting when operating in the module mode.

PRGM Store - Programs all front panel control switch settings into the program module at the location indicated by the program number switch when operating in the module mode.

Power - Turns on and off main power to the instrument.

## 3. MICROPROCESSOR SYSTEM

The schematics for the 8085-based microprocessor system and remote interface are shown in Figures 3, 4, 5, and 6. The system was designed and constructed at the beginning of the program, and had been utilized as a valuable design tool for checkout of all microprocessor-controlled circuitry. The central processing section, shown in

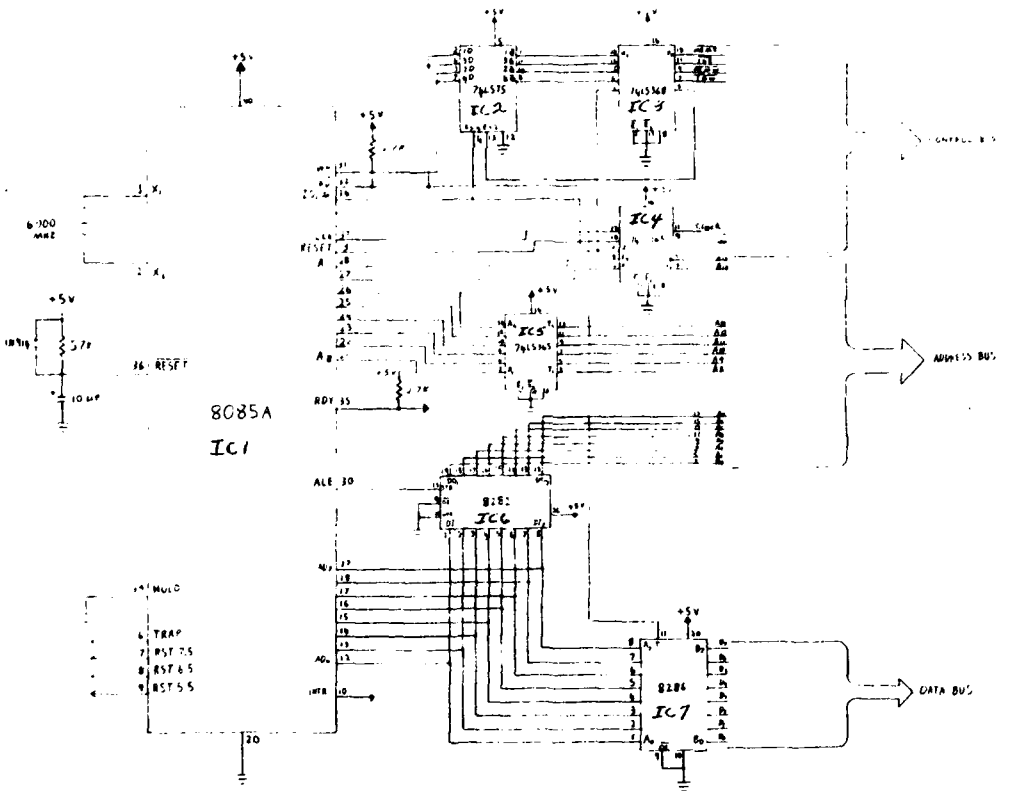


Figure 3. Central Processing System Schematic

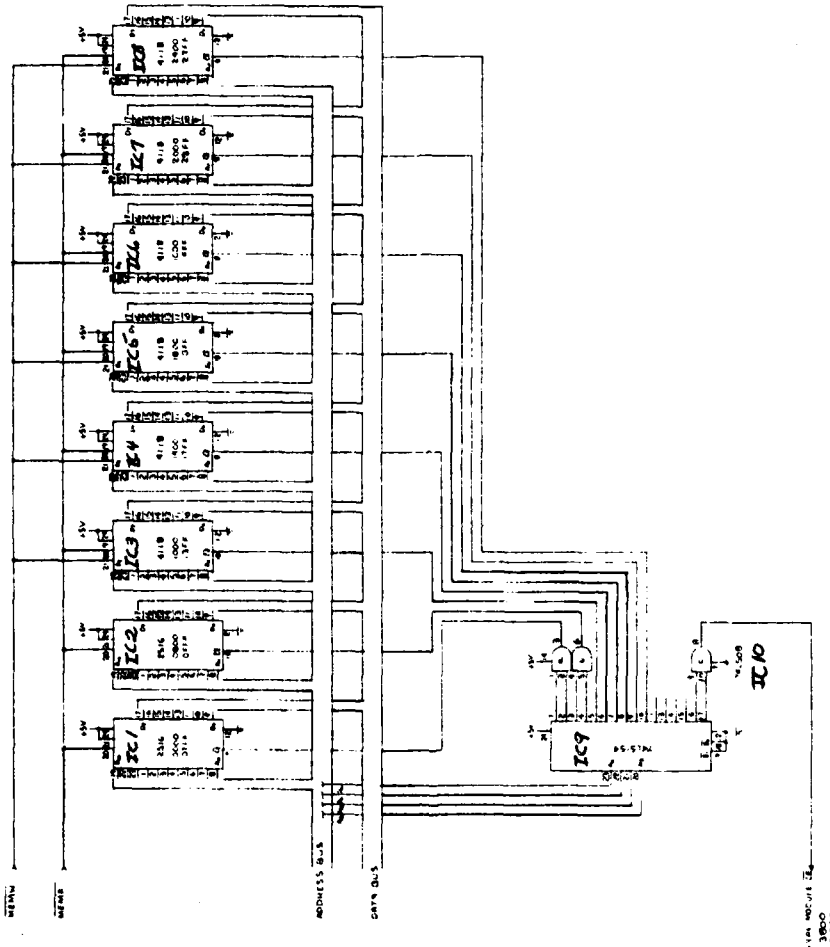


Figure 4. Memory System Schematic

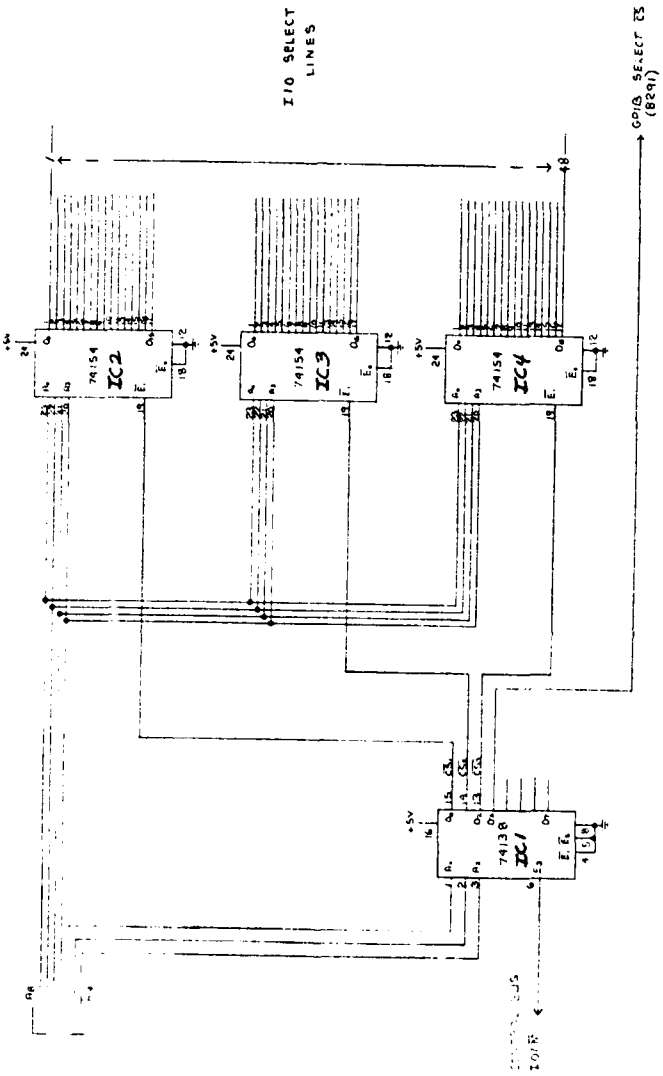


Figure 5. Port Selection System Schematic

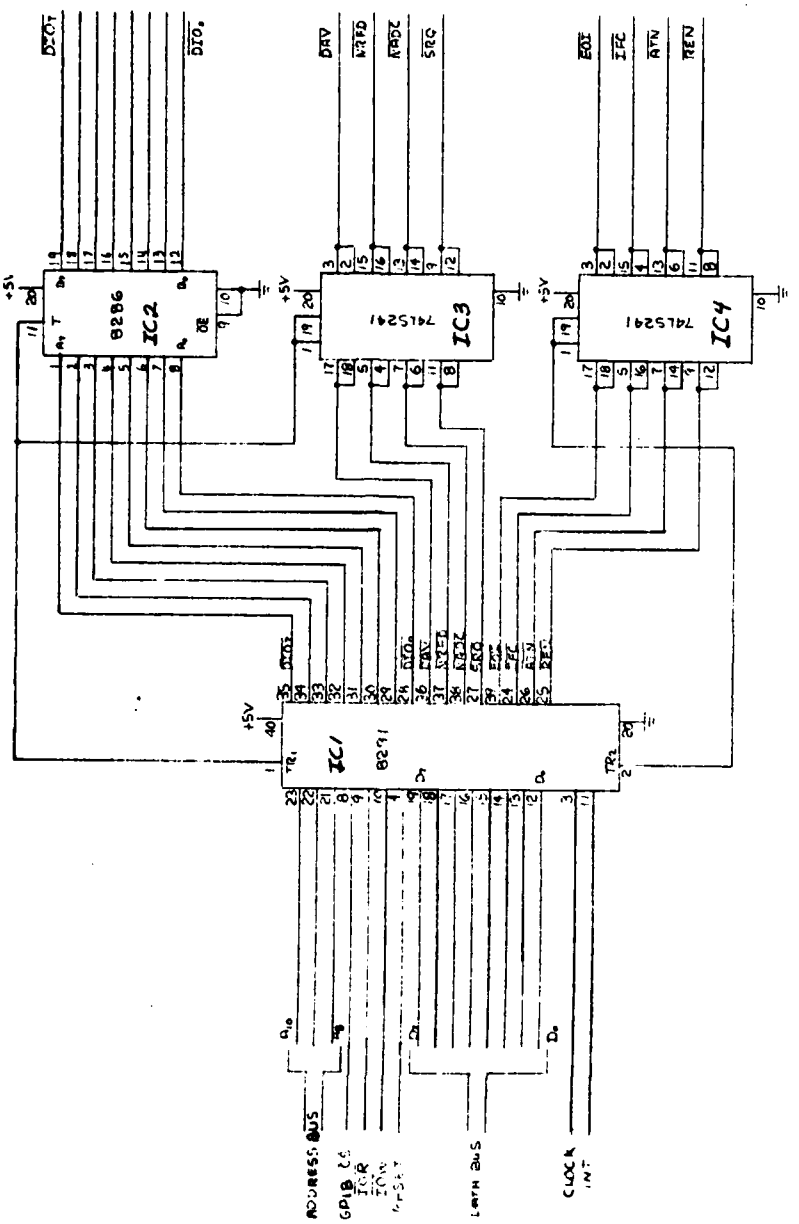


Figure 6. GPIB Interface Schematic

Figure 3, has an 8-bit bidirectional data bus, a 16-bit address bus, and an 8-bit control bus. The internal clock rate of the 8085 processor has been set to 3 MHz. The memory section is shown in Figure 4. The design includes the capability for 4K of program storage and 6K of data storage. The central processor has the capability of selecting 1 of 48 I/O ports as shown in Figure 5. Each i/O port corresponds to a control function on the front panel or internal to the unit. The schematic shown in Figure 6 is the control circuitry for the remote interface. The 8291 remote interface processing unit has been designed by the Intel Corporation to conform to the IEEE-488 general purpose instrumentation interface standard. The microprocessor system has been designed onto a printed circuit board. The complete microprocessor system is shown in Figure 7.

## 4. PROGRAM MODULE

The schematic and timing diagram for the program module is shown in Figures 8 and 9, respectively. The basis for the nonvolatile storage of the front panel control functions is the TMS-2516, electrically programmable read only memory (EPROM). The EPROM is mounted into a modular container that plugs into the front panel, and can store up to 100 complete programs. A program consists of storing the control codes for each of the 14 front panel controls.

The operation of the program module is initiated by inserting the module into the front panel slot and pushing the reset button. This action will load all the contents of the EPROM into the system memory. The program number is then selected and the module mode select switch pushed. The contents of the program selected will set all the front panel control functions to the preprogrammed settings. The front panel displays will now correspond to the stored control functions and not the switches on the front panel. The stored programs may be erased by removing the program module and exposing it to an ultraviolet light. Once the program module is subjected to a wavelength of 2537 angstroms for 21 minutes, it can be reinserted into the unit for programming.

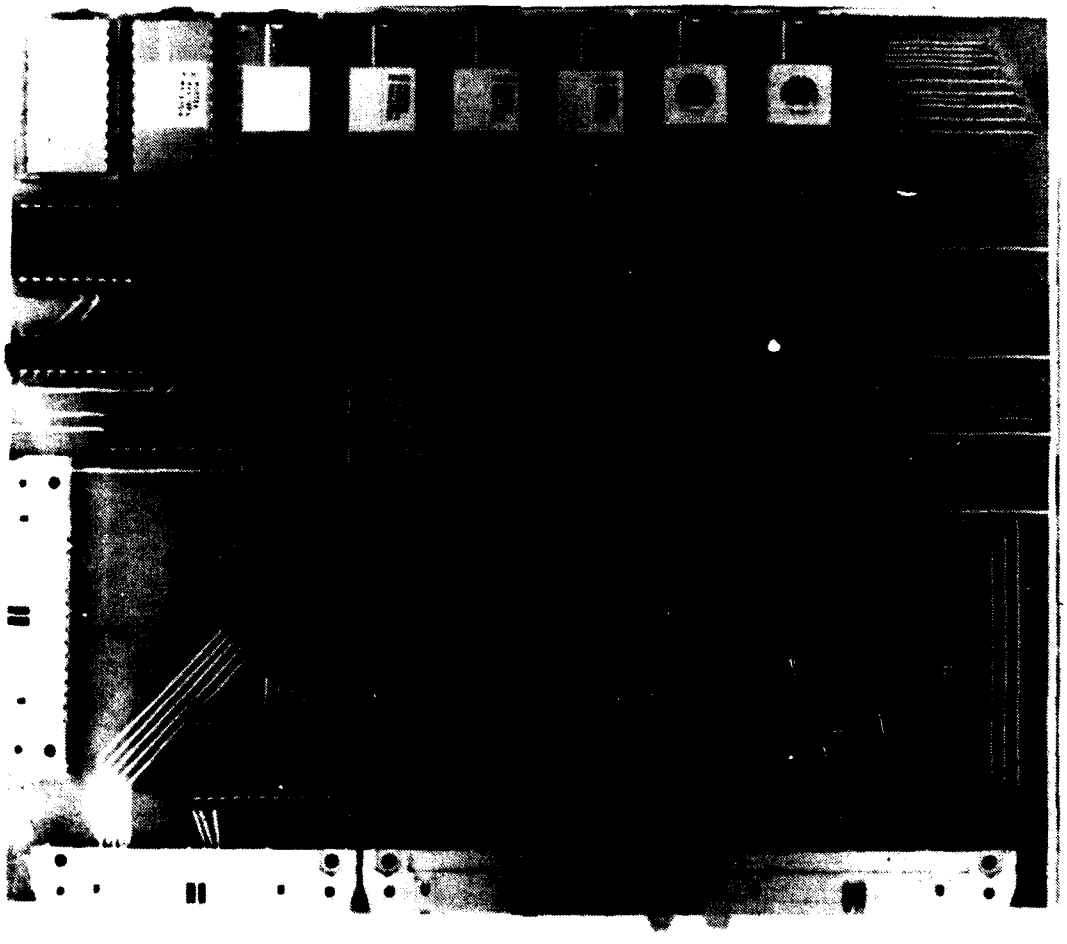

Figure 7. 8085 Microprocessor System

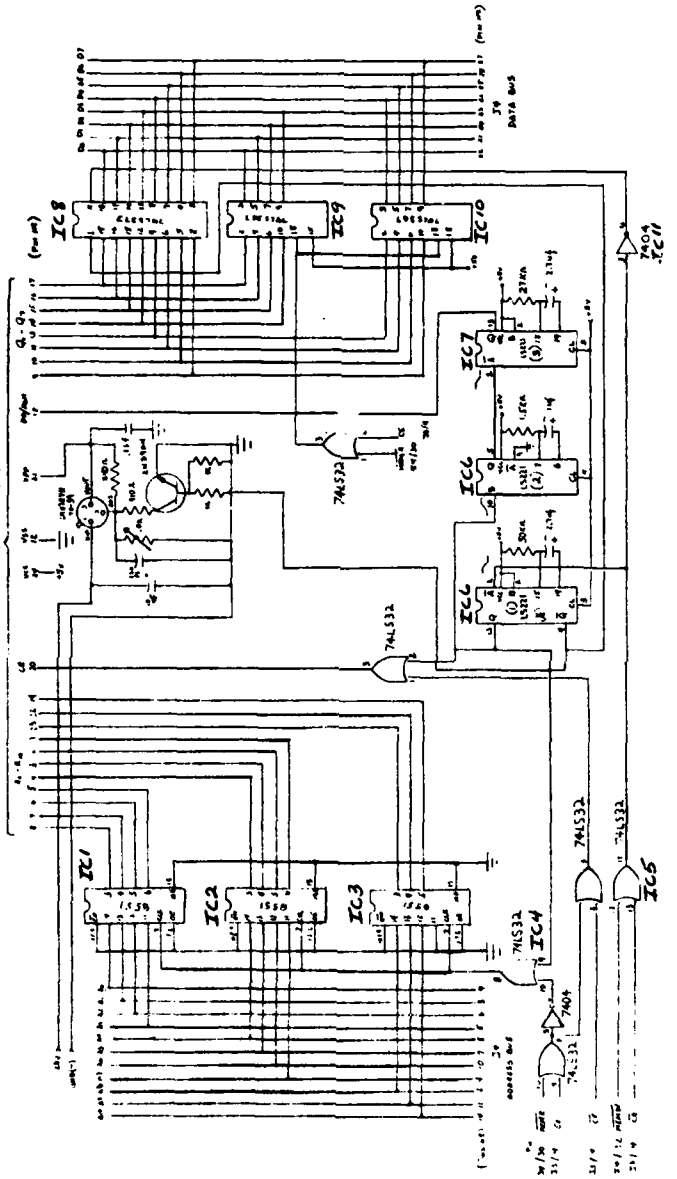


Figure 8. Program Module Interface Schematic

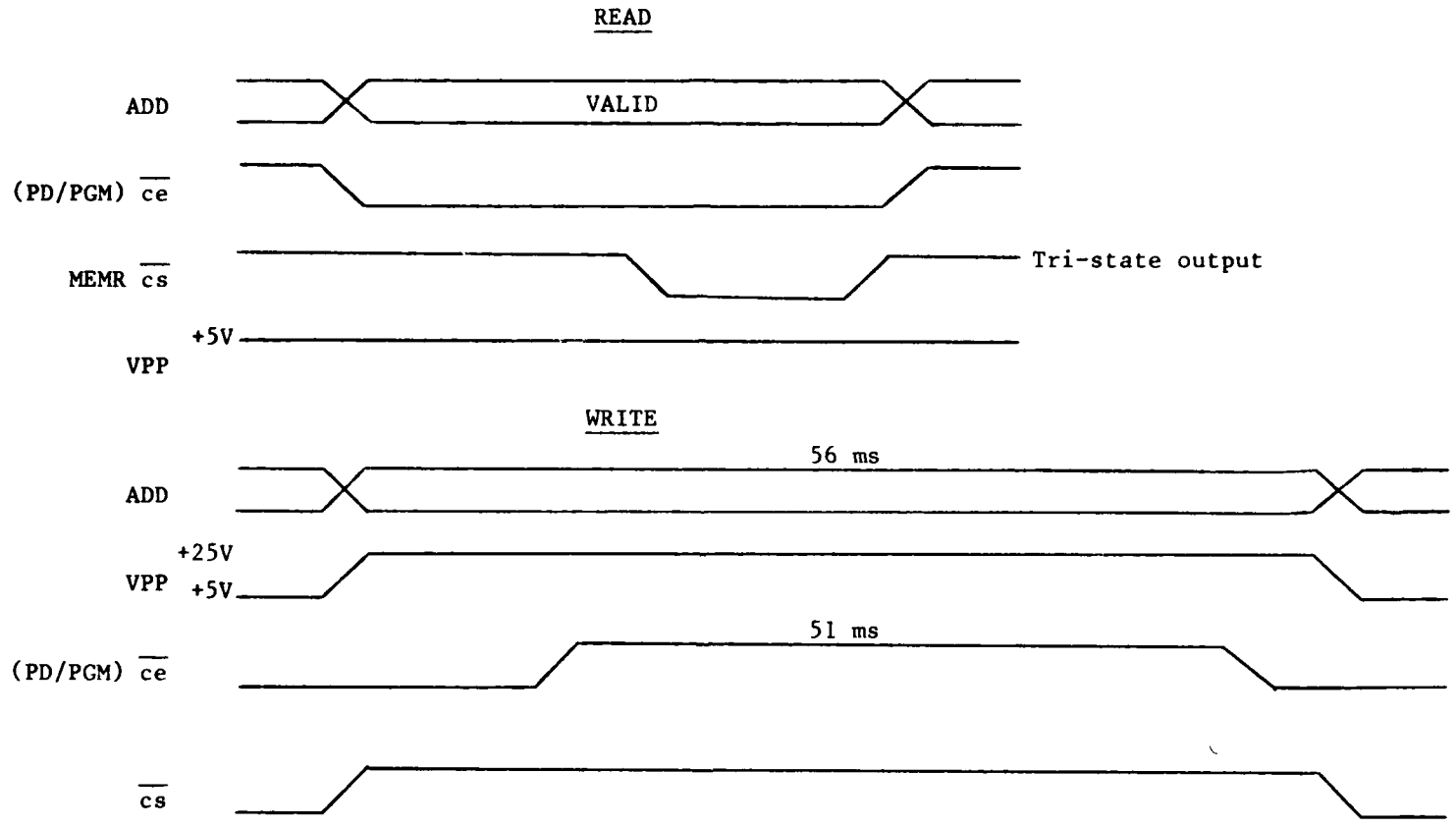


Figure 9. Program Module Timing Diagram

The programming of the program module is accomplished by the EPROM programming circuitry shown in Figure 8. The circuitry receives the data and control pulses from the microprocessor system. Again, this manipulation of data can only be achieved with the use of the microprocessor incorporated into the system. The operator will select the desired changes in the program via the front panel controls. He then unlocks the module safety switch and pushes the alter button. The altered program or programs will then be automatically programmed onto the erased EPROM. The program module and circuit board are shown in Figure 10, before encapsulation.

5. PRF GENERATOR

The PRF Generator is designed for use with the microprocessor system. Its purpose is to generate the pulser/receiver timing frequencies from 10 Hz to 9.99 KHz with a 10 Hz resolution.

The PRF Generator schematic, as shown in Figure 11, consists of five data hold latches, five presetable counters, and one 10 MHz crystal clock oscillator. The crystal oscillator (10 MHz) determines the 10 Hz resolution, and the presetable counters determine the frequency range.

When in the local mode, the microprocessor reads the state of the PRF select switches on the front panel. When in the programmable module mode, the microprocessor reads from a memory location. The information is then converted to the PRF Generator coding by the software implementation of the algorithm, shown below:

$$P = 1/F/200 \times 10^{-9} \qquad (1)$$

Where: $P$ = PRF Generator coding

$F$ = PRF selected

$200 \times 10^{-9}$ = clock period $\times$ 2

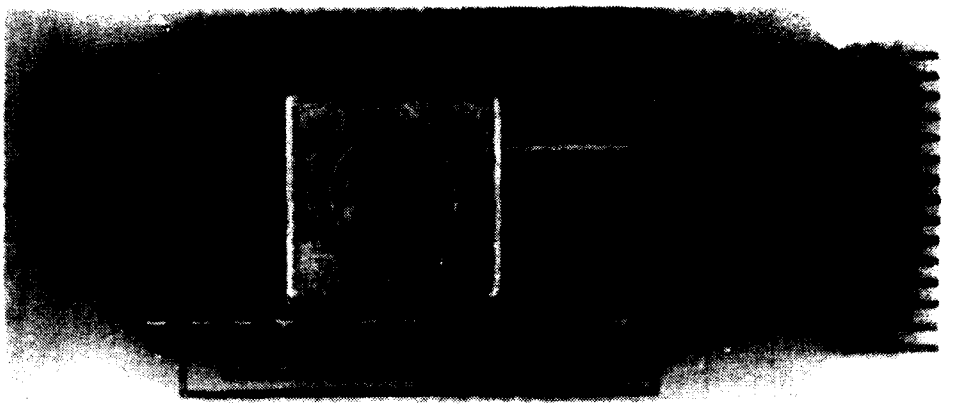

Figure 10a. Program Module and Circuit Board, Enlarged

Figure 10b. Program Module and Circuit Board, Actual Size

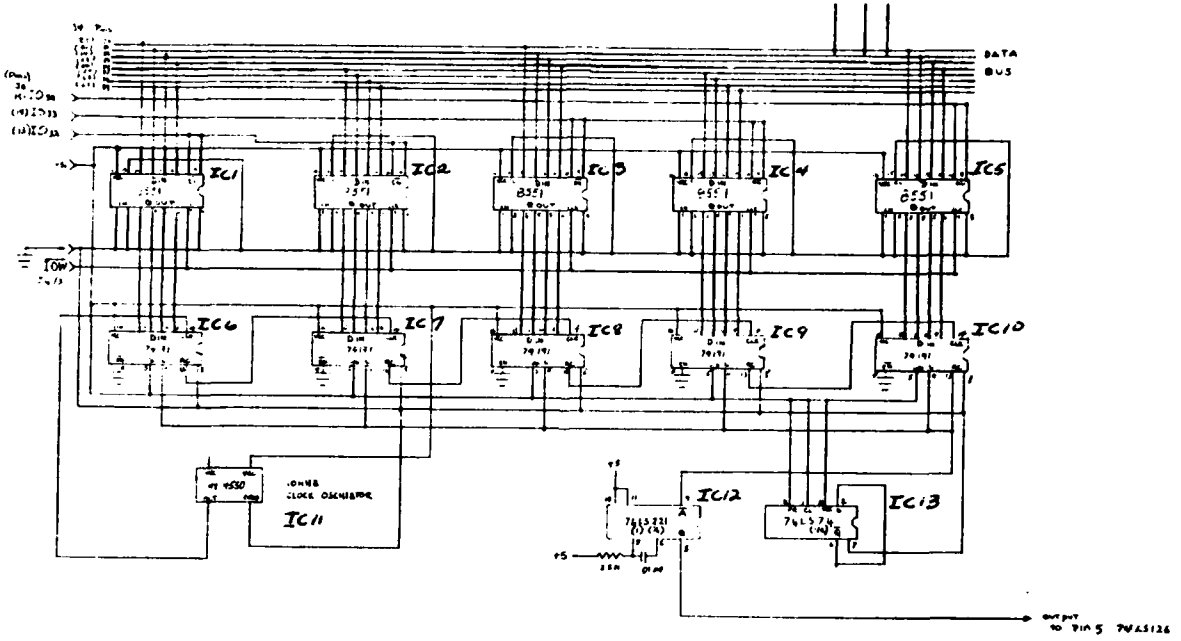


Figure 11. PRF Generator Schematic

A software calibration routine has been developed to eliminate generator coding errors introduced by the rounding off of the results of the algorithm when converting it to its binary equivalent.

## 6. PRF COUNTER

An important feature of the PRF Generator System is that it is self-calibrated. By this we mean that when the PRF generator is in use, a frequency (PRF) counter measures its output, and the microprocessor monitors both the PRF selected and the output given by the PRF counter. In this way, malfunctions and errors are detected by the microprocessor which, in turn, advises the user/operator of the condition.

The PRF counter schematic, as shown in Figure 12, utilizes the ICM7226A Universal Counter Integrated Circuit. The accuracy of the circuit is preset during a hardware calibration procedure. The output of the counter is read by the microprocessor and compared to the selected PRF. If the comparison is within the 10 Hz tolerance, the microprocessor will display the PRF that was selected. If the comparison shows an error condition, the microprocessor will implement a calibration routine until the PRF counter is within the tolerance specified.

The PRF counter input is automatically switched to the synchronization input when the PRF switch is placed in the 000 Hz position. The microprocessor will then be able to read the frequency of the synchronization input and display the measurement on the front panel. A software routine has been added that will inhibit the external synchronization frequency if it exceeds 9.99 KHz. The control will automatically switch to internal and the PRF will be set to 9.99 KHz.

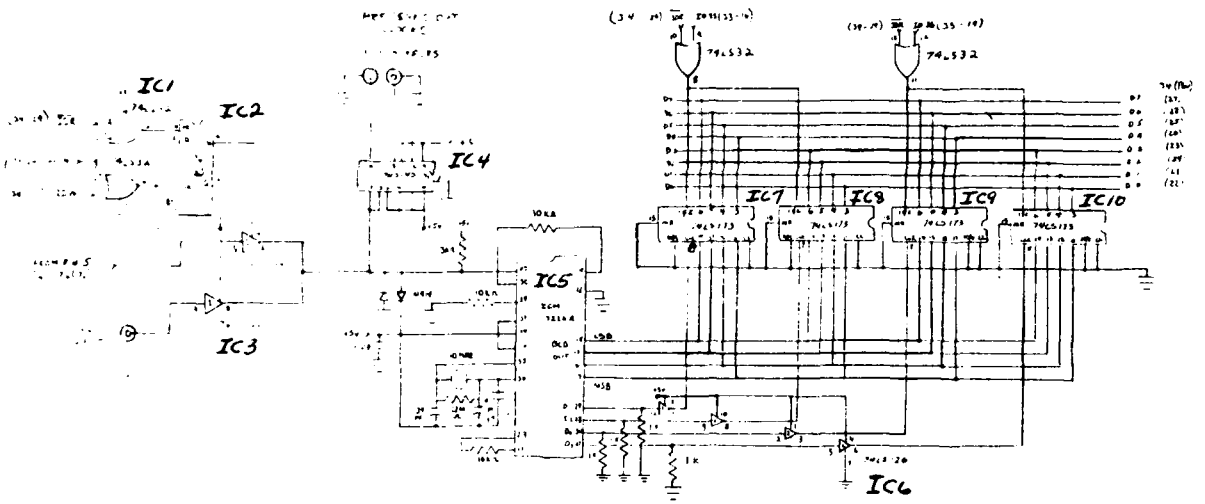


Figure 12. PRF Counter Schematic

## 7. PREAMPLIFIER

The RF preamplifier, as shown in Figure 13, has been specifically designed for this application using discrete components and a modular technique. It was determined early in the program that commercially built integrated circuits did not conform to the high performance specifications needed to comply with the program specifications. Figure 14 shows the completed module.

The design incorporates FET transistors in the amplifier sections for fast recovery and wide bandwidth capabilities. The amplifier has a 50 ohm input and output impedance for compatibility with coaxial cable systems. This feature reduces system noise and eliminates high gain oscillations.

The preamplifier design was evaluated with the use of a Hewlett Packard Generator/Sweeper, Model Number 8601A, and a Tektronix Spectrum Analyzer, Model Number 7L12. A swept cw signal, .5 MHz to 100 MHz, was introduced at the input to the preamplifier at a specified power level. The signal at the output was then fed to the spectrum analyzer where the amplitude response as a function of frequency was recorded. Data points at specific frequencies were recorded to yield Table 1. This table shows the compiled data of the input power (dBm) versus the resultant output power (dBm). Figure 15 shows the plot of output power (dBm) versus frequency (MHz) using the data from Table 1.

Plots were made of input versus output power at a single frequency. The -3 dB compression point, noise floor, dynamic range, gain, and linearity can all be determined as shown in Figures 16 through 20.

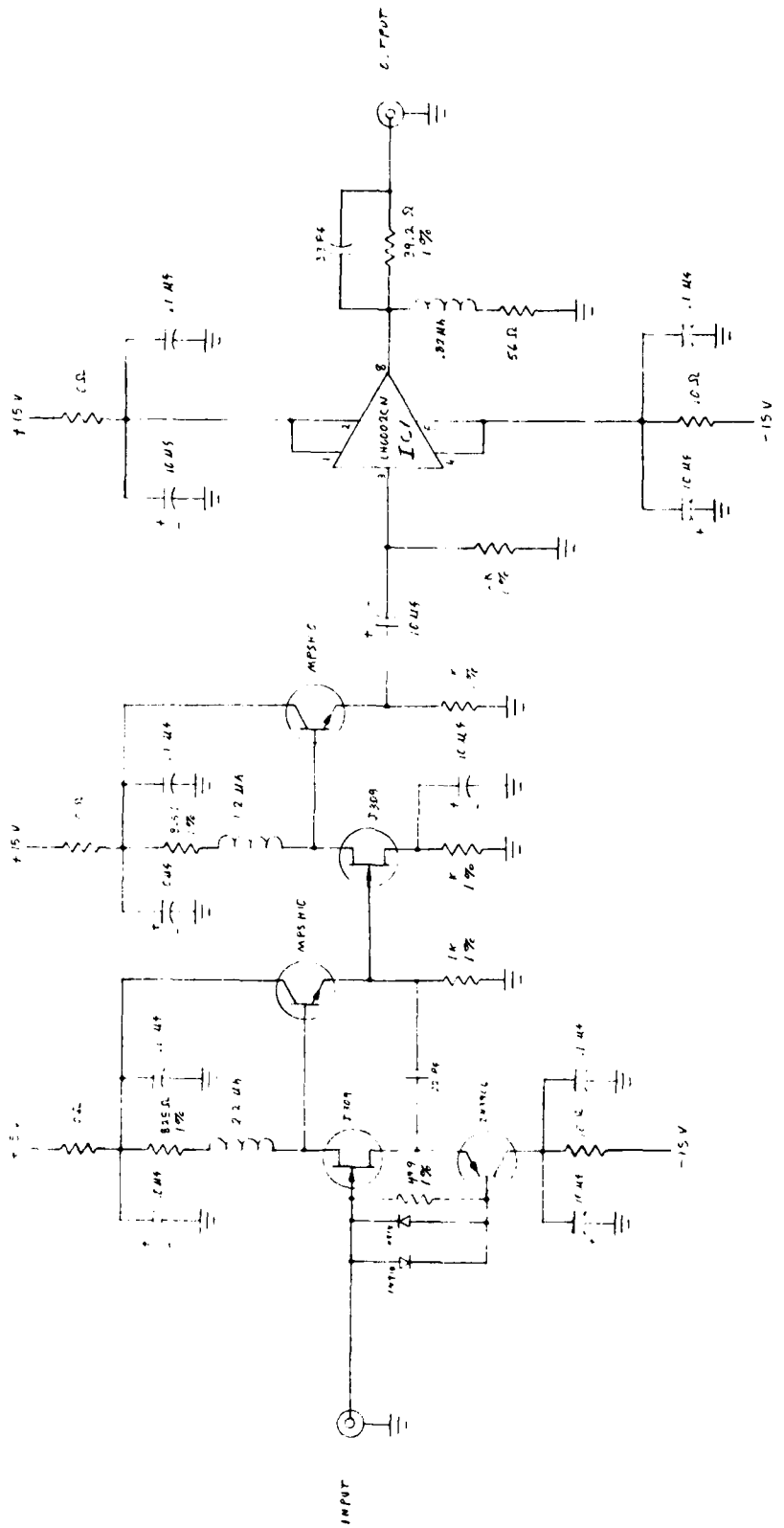

Figure 13. Preamplifier Schematic

Internal

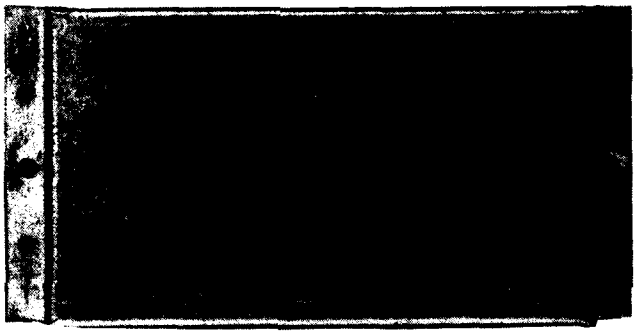

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Figure 14. Preamplifier Module

TABLE 1

PREAMPLIFIER EVALUATION DATA

| Input Power (dBm) | -1 | -11 | -21 | -31 | -41 | -51 | -61 | -71 | -81 | -93 | -103 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | RESULTANT OUTPUT POWER (dBm) | | | | | | | | | | |
| Frequency (MHz) | | | | | | | | | | | |
| .5 | 17.0 | 14.6 | 8.6 | -.6 | -10.8 | -20.6 | -30.8 | -40.6 | -50.6 | -61.2 | -67.0 |
| 5.0 | 15.0 | 14.6 | 8.6 | -.6 | -10.8 | -20.6 | -30.8 | -40.6 | -50.6 | -61.2 | -67.0 |
| 10.0 | 14.5 | 14.6 | 8.6 | -.6 | -10.8 | -20.6 | -30.8 | -40.6 | -50.6 | -61.2 | -67.0 |
| 15.0 | 13.4 | 14.6 | 8.6 | -.6 | -10.8 | -20.6 | -30.8 | -40.6 | -50.6 | -61.2 | -67.0 |
| 20.0 | 12.4 | 14.4 | 8.6 | -.6 | -10.8 | -20.6 | -30.8 | -40.6 | -50.6 | -61.2 | -67.0 |
| 25.0 | 12.0 | 13.6 | 8.6 | -.6 | -10.8 | -20.6 | -30.8 | -40.6 | -50.6 | -61.2 | -67.0 |
| 30.0 | 11.4 | 13.0 | 8.6 | -.6 | -10.8 | -20.6 | -30.8 | -40.6 | -50.6 | -61.2 | -67.0 |
| 35.0 | 10.6 | 12.4 | 8.5 | -.7 | -10.9 | -20.8 | -30.8 | -40.6 | -50.6 | -61.2 | -67.0 |
| 40.0 | 10.2 | 11.6 | 8.4 | -.8 | -11.0 | -20.9 | -30.8 | -40.6 | -50.6 | -61.2 | -67.0 |
| 45.0 | 9.6 | 10.6 | 8.3 | -1.0 | -11.1 | -21.0 | -30.9 | -40.7 | -50.6 | -61.6 | -67.2 |
| 50.0 | 9.0 | 10.0 | 8.0 | -1.2 | -11.2 | -21.2 | -31.0 | -40.8 | -50.6 | -61.8 | -68.4 |
| 55.0 | 8.6 | 9.2 | 7.6 | -1.5 | -11.6 | -21.6 | -31.6 | -41.0 | -51.0 | -62.0 | -68.6 |
| 60.0 | 8.0 | 8.5 | 7.0 | -1.9 | -12.0 | -22.0 | -31.9 | -41.8 | -51.6 | -62.4 | -69.0 |
| 65.0 | 7.6 | 7.8 | 6.4 | -2.4 | -12.5 | -22.5 | -32.4 | -42.4 | -52.0 | -62.8 | -69.6 |
| 70.0 | 7.0 | 7.4 | 5.6 | -3.0 | -13.0 | -23.0 | -33.0 | -43.0 | -52.6 | -63.2 | -69.8 |
| 75.0 | 6.6 | 6.6 | 5.0 | -3.6 | -13.6 | -23.6 | -33.6 | -43.6 | -53.2 | -64.0 | -70.0 |
| 80.0 | 6.0 | 6.2 | 4.4 | -4.0 | -14.1 | -24.0 | -34.4 | -44.1 | -54.0 | -64.8 | -70.8 |
| 85.0 | --- | --- | 3.7 | -4.5 | -14.7 | -24.4 | -34.8 | -44.6 | -54.4 | -65.0 | -71.4 |
| 90.0 | --- | --- | 3.1 | -4.8 | -14.8 | -24.8 | -35.0 | -45.0 | -54.8 | -65.6 | -71.8 |
| 95.0 | --- | --- | 2.6 | -4.9 | -15.0 | -24.9 | -35.0 | -45.0 | -55.0 | -65.6 | -72.0 |
| 100.0 | --- | --- | 2.4 | -5.0 | -15.0 | -24.9 | -35.0 | -45.0 | -55.0 | -65.6 | -72.0 |

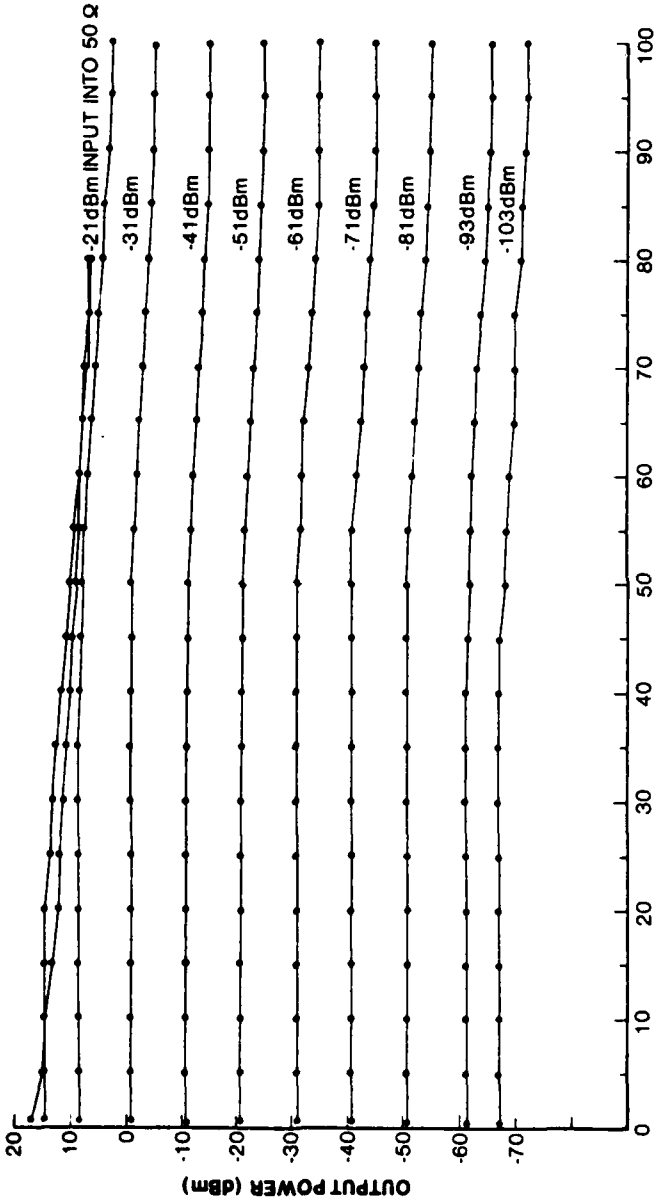



Figure 15. Preamplifier Evaluation Plot of Output Power Versus Frequency

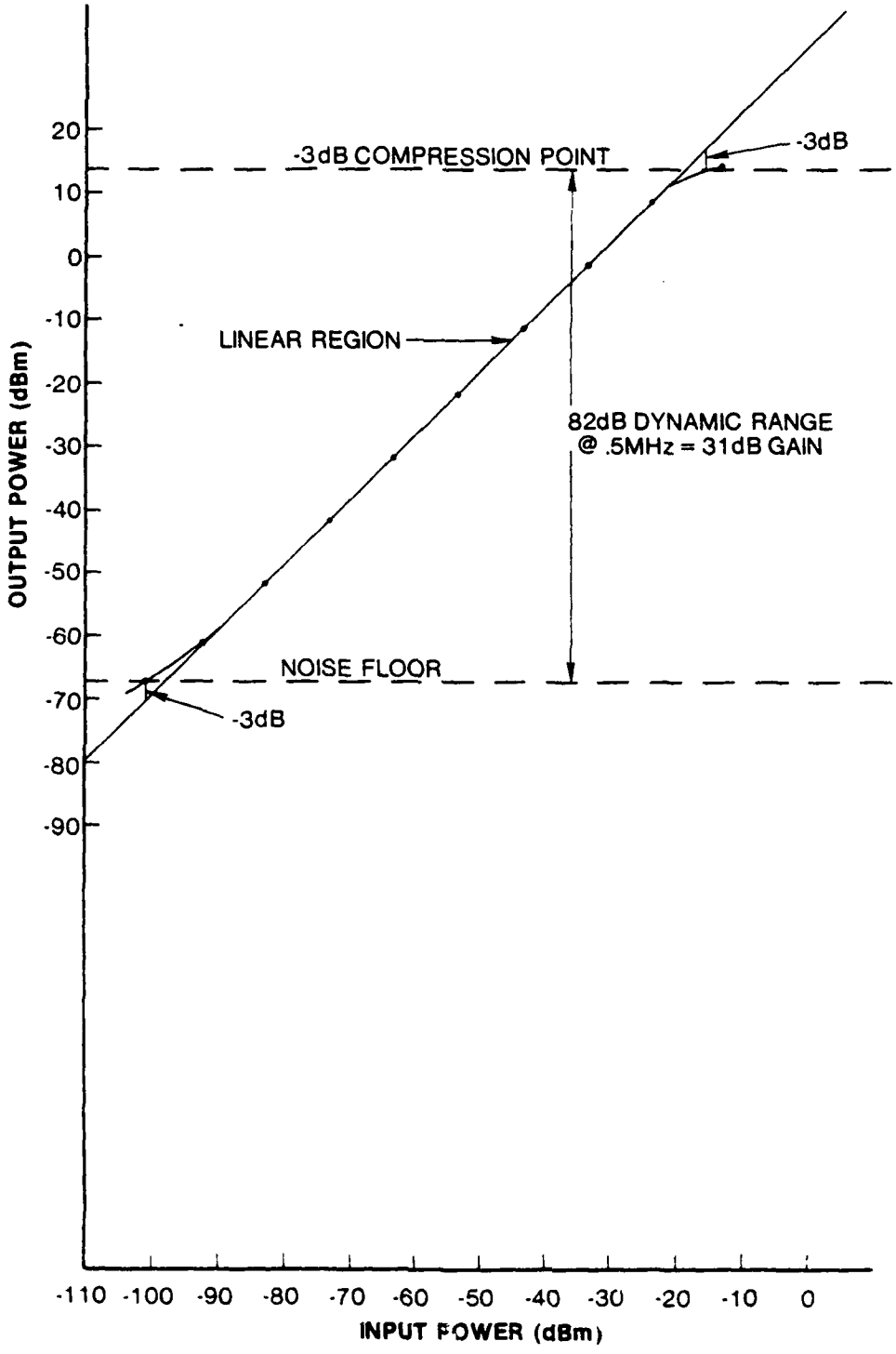



Figure 16. Preamplifier Evaluation Plot of Output Power Versus Input Power at .5 MHz

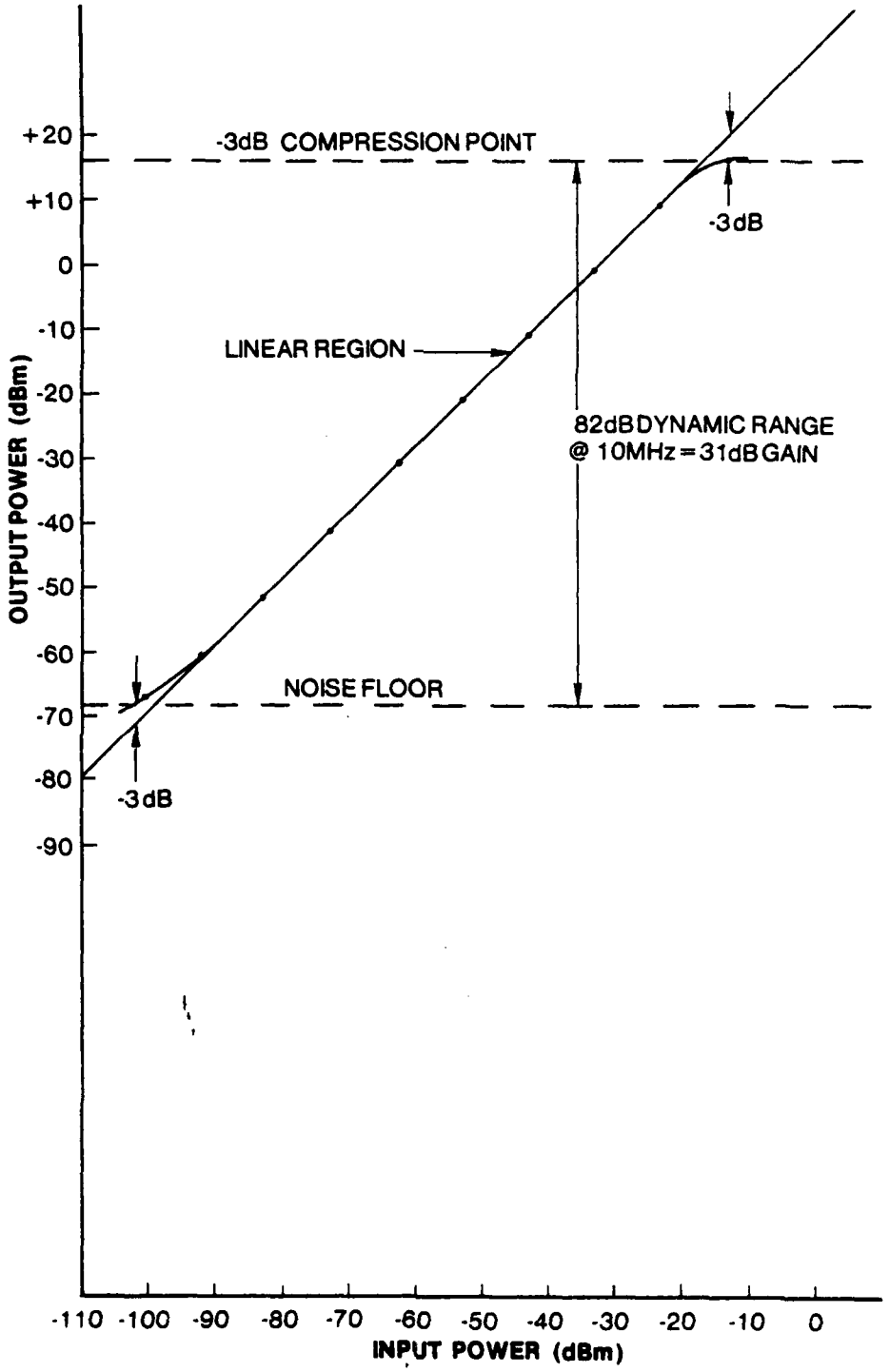



Figure 17. Preamplifier Evaluation Plot of Output Power Versus Input Power at 10 MHz

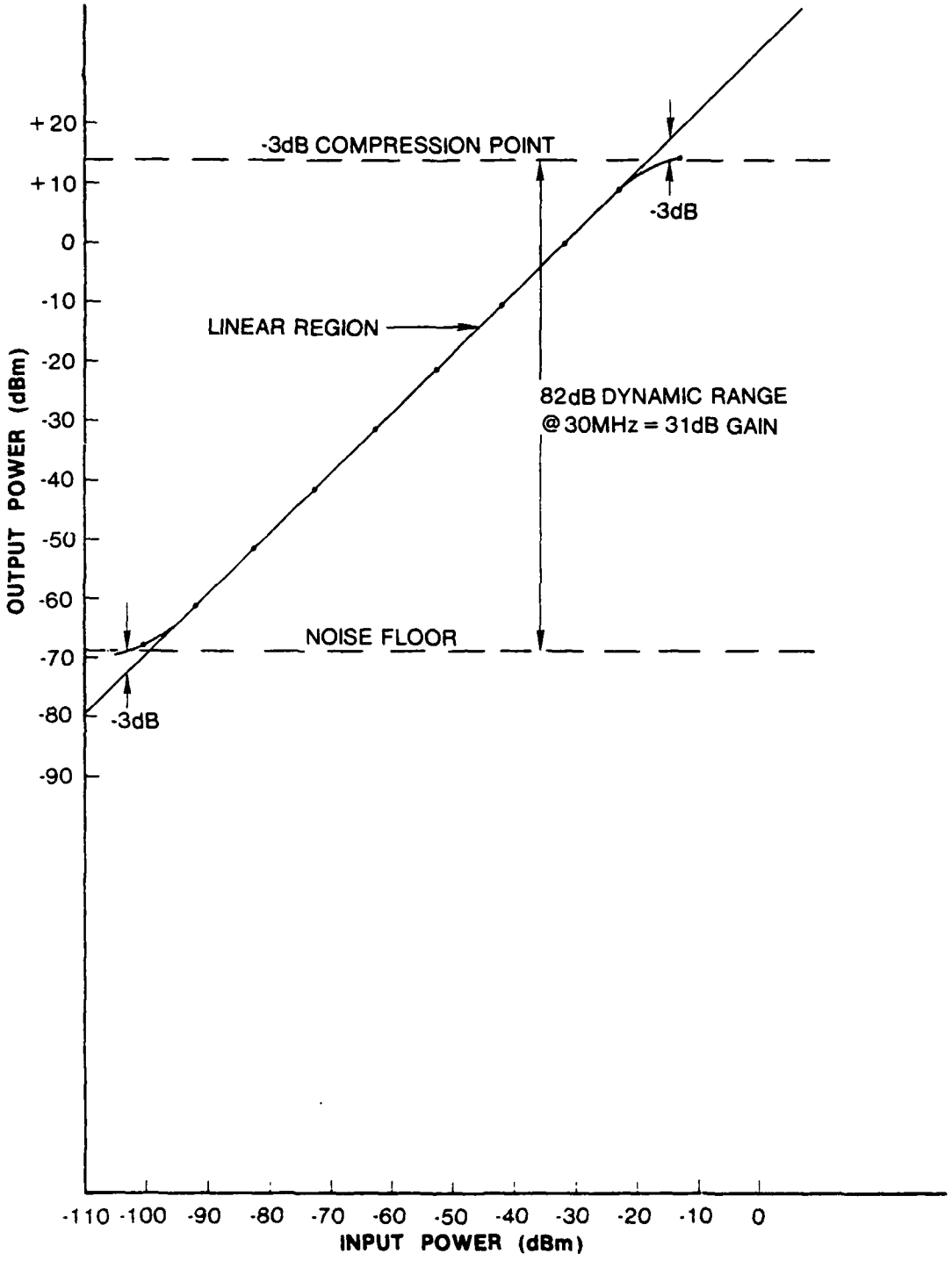



Figure 18. Preamplifier Evaluation Plot of Output Power Versus Input Power at 30 MHz

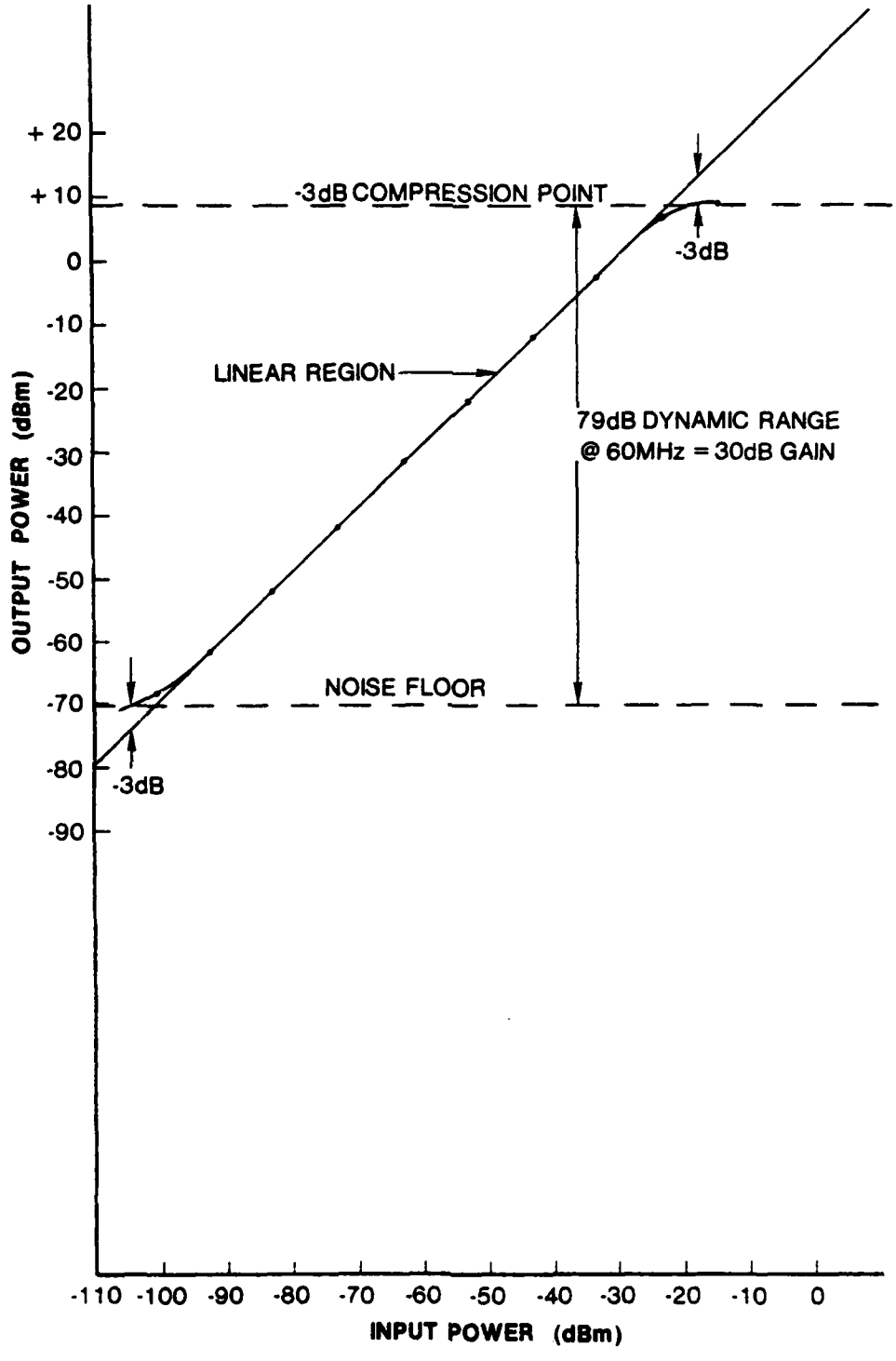



Figure 19. Preamplifier Evaluation Plot of Output Power Versus Input Power at 60 MHz

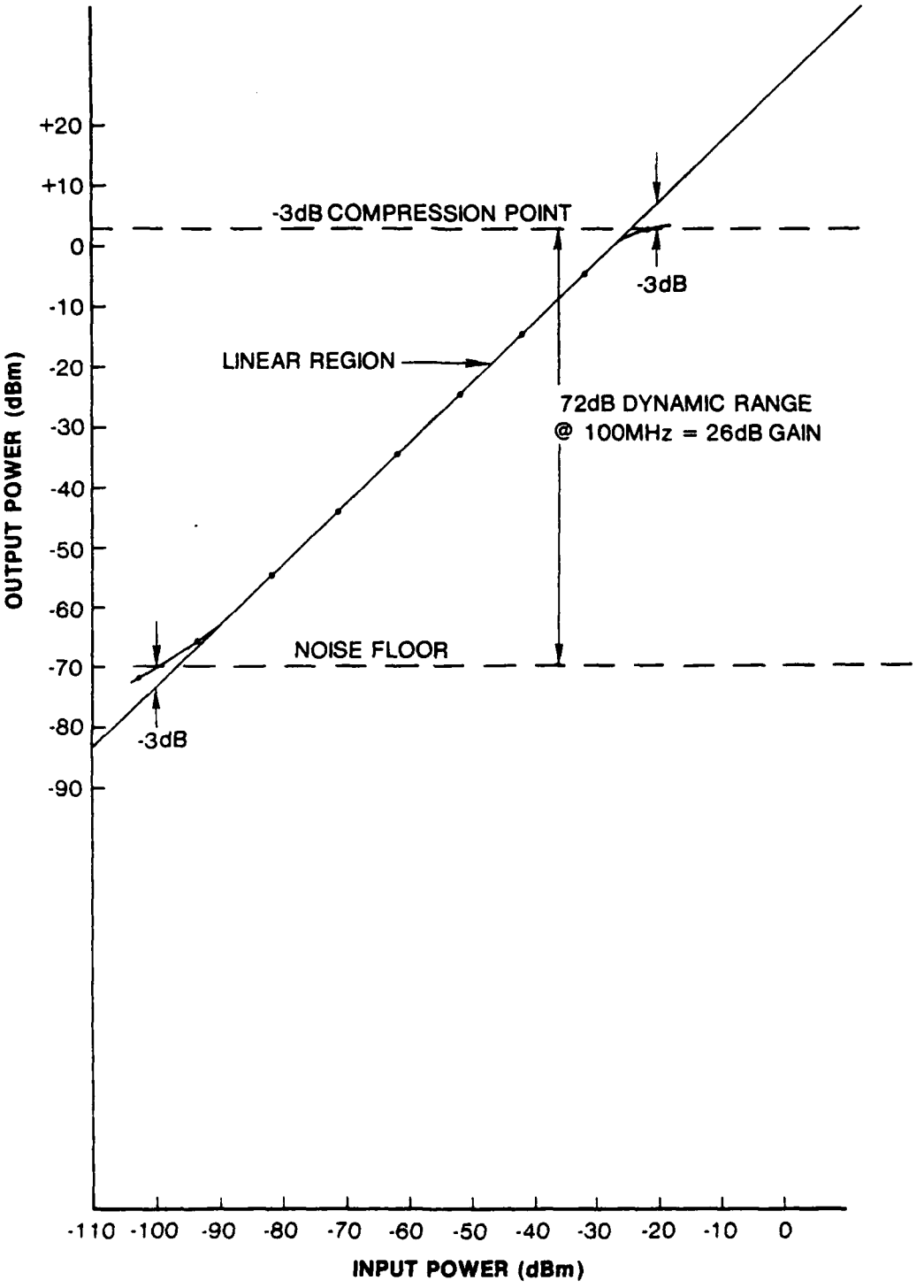



Figure 20. Preamplifier Evaluation Plot of Output Power Versus Input Power at 100 MHz

The basic linear expression for the gain curve is

$$P_{out} = G\ P_{in} \tag{2}$$

Taking the $\log_{10}$ of both sides of the expression and then multiplying both sides by 10 results in the expression

$$10\ \mathrm{Log}_{10}\ P_{out} = 10\ \mathrm{Log}_{10}\ P_{in} + 10\ \mathrm{Log}_{10}\ G \tag{3}$$

If the amplitude of both input and output powers are measured and plotted in dB, the following linear expression with a slope of 1 results:

$$P_{out} = P_{in} + G \tag{4}$$

The preamplifier was found to have measured a bandwidth of ≥60 MHz at ±0.5 dB as shown in Figure 15. The dynamic range at 60 MHz was 79 dB with a gain of 30 dB (see Figure 19). The preamplifier will operate up to 100 MHz with a dynamic range of 72 dB and a gain of 26 dB.

## 8. VARIABLE GAIN AMPLIFIER

The variable gain amplifier schematic, shown in Figure 21, was designed to control the amplitude of the RF signal. The gain is controlled by a dc level or sinusoidal function generated by the controlling microprocessor. The amplifier is a modular design with 30 dB of gain control. Amplifier modules may be connected in series for a total accumulative gain control. The amplifier will replace large and expensive relay attenuators. Figure 22 shows the gain control interface schematic and Figure 23 shows the completed module.

The gain (dB) versus control voltage (volts) was evaluated with the use of the Hewlett Packard Generator/Sweep and the 250 MHz Tektronix Oscilloscope. A cw signal was introduced to the input to the

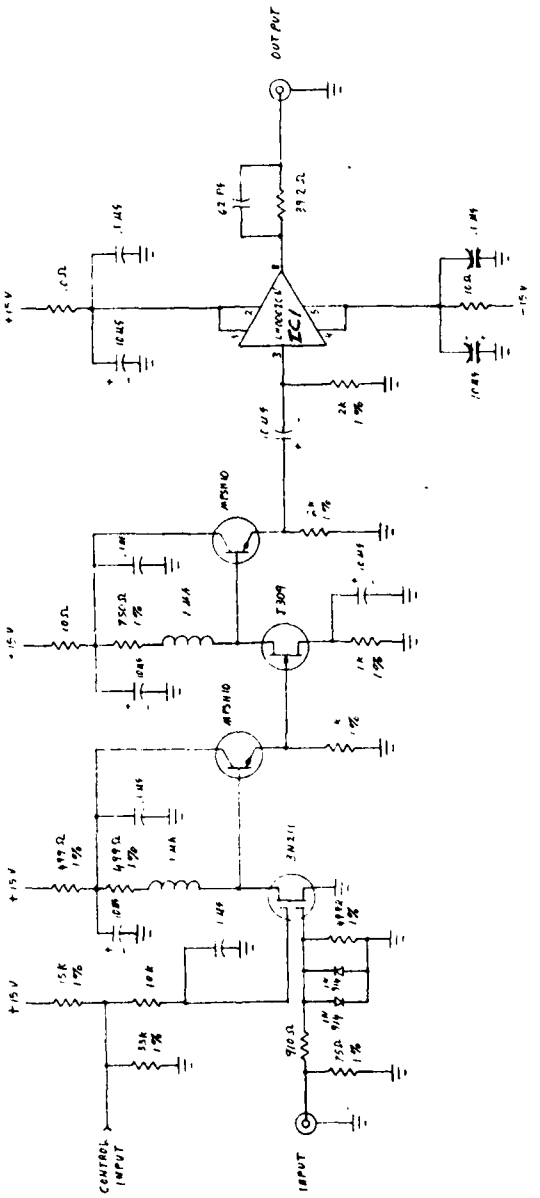



Figure 21. Variable Gain Amplifier Schematic

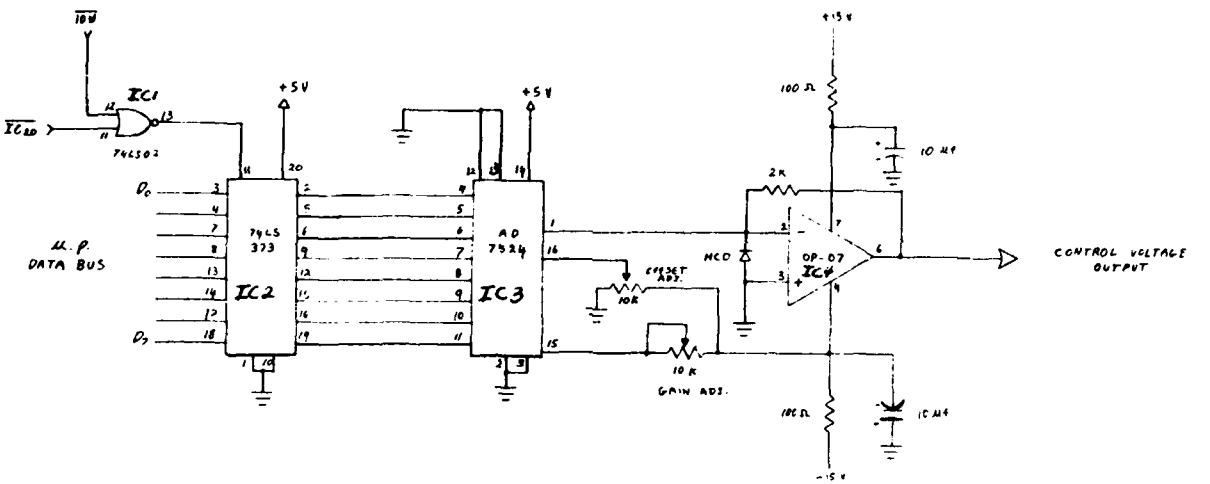



Figure 22. Variable Gain Amplifier Control Schematic

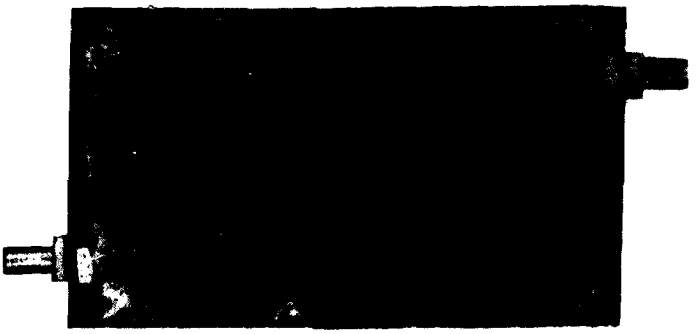


Figure 23. RF Variable Gain Amplifier Module

amplifier and the output fed to the oscilloscope. The output amplitude was measured for each variation in control voltages and the results plotted on the graphs as shown in Figures 24 through 27. The complete gain/volts measurements were plotted for 1 MHz, 10 MHz, 30 MHz, and 60 MHz input frequencies. The results show a linear gain control function that can be implemented by the microprocessor.

The variable gain amplifier was evaluated for the -3 dB compression point, noise floor, dynamic range, gain, and linearity as previously described for the preamplifier. Table 2 and Figures 28 through 33 show a measured bandwidth of ≥60 MHz at ±0.5 dB and a dynamic range of 60 MHz of 75 dB with a gain of 29.5 dB. The amplifier will operate up to 100 MHz with a dynamic range of 75 dB and a gain of 24 dB.

## 9. LOGARITHMIC AMPLIFIER

The schematic of the logarithmic amplifier is shown in Figure 34. The design incorporates Texas Instrument's TL441 logarithmic section as the linear to logarithmic conversion device. This logarithmic device has four 30 dB sections designed into it for a total theoretical input dynamic range of 120 dB.

The first design of the logarithmic amplifier incorporated all four sections. The circuit configuration produced incurable oscillations. The second and final design, shown in Figure 34, incorporates three logarithmic sections for a theoretical input dynamic range of 90 dB. In actual testing, the measured input dynamic range proved to be approximately 80 dB. The diagrams shown in Figures 35 through 40 are the results from the testing of this circuit. The logarithmic amplifier was tested at the frequencies of 5, 10, 15, 20, 25, and 30 MHz. It must be noted that although the TL441 logarithmic device frequency specifications say that the high end frequency range is to be 40 MHz, testing has found that the output amplitude reduces after 30 MHz.

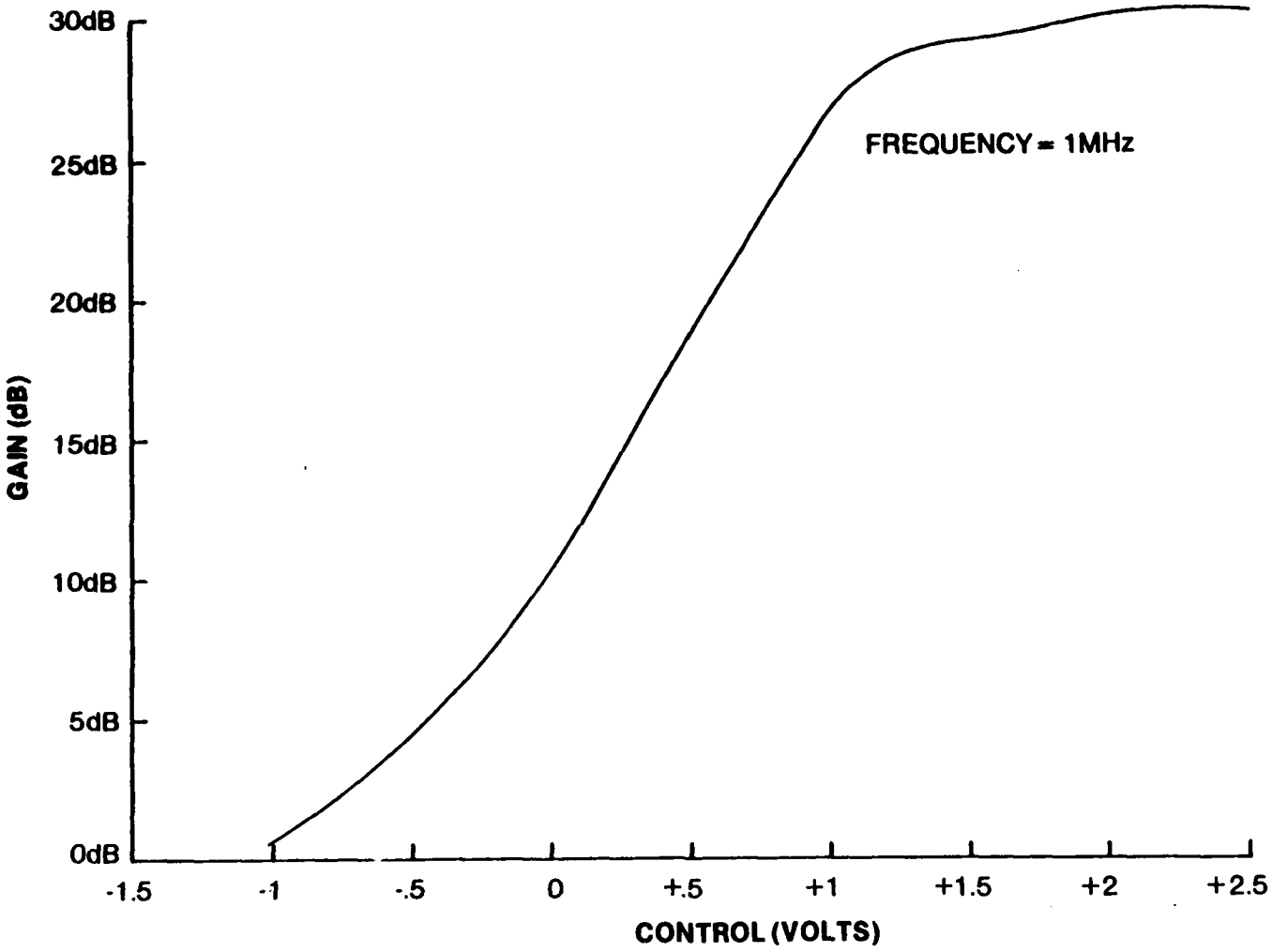



Figure 24. Variable Gain Amplifier Plot of Gain Versus Control Volts at 1 MHz

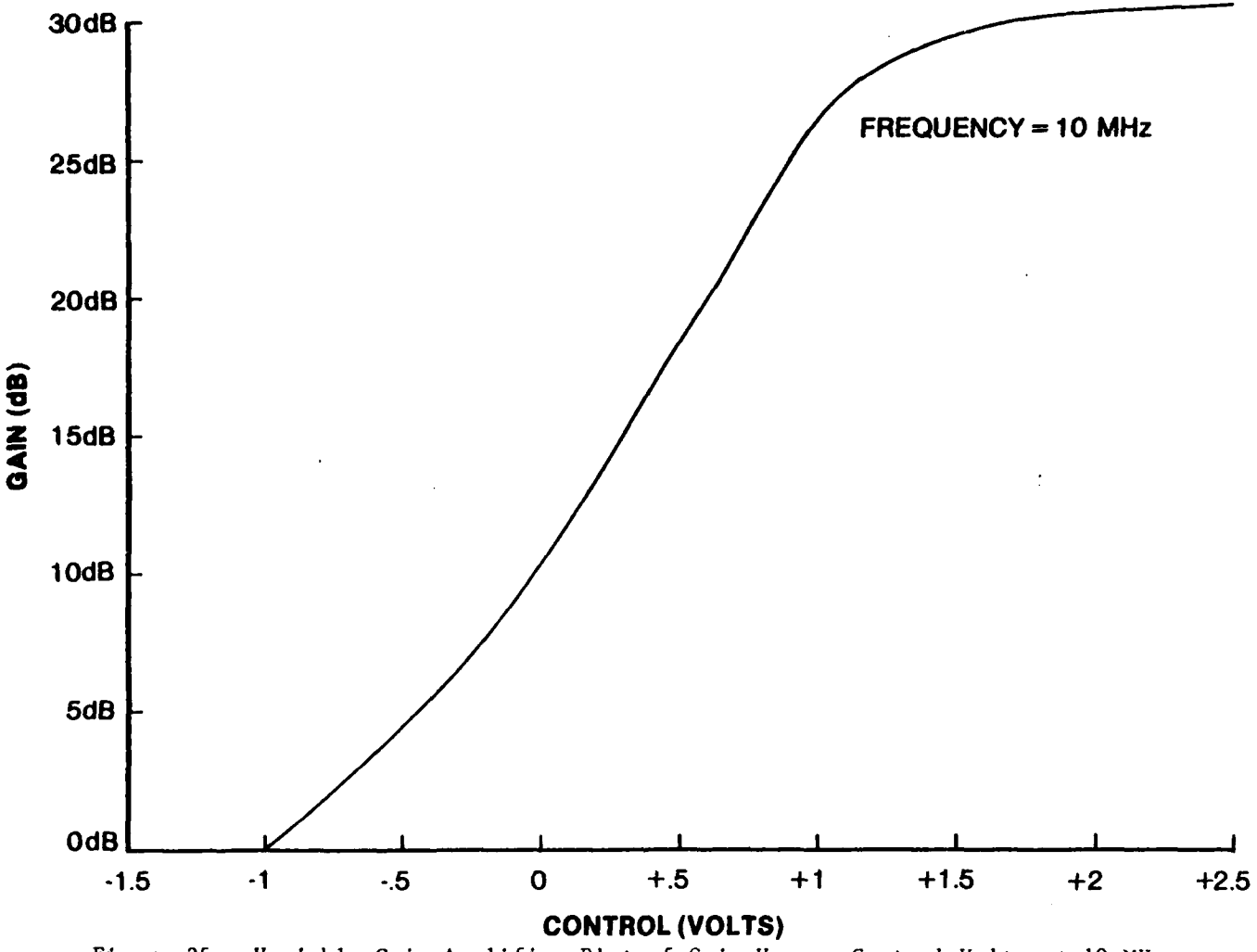



Figure 25. Variable Gain Amplifier Plot of Gain Versus Control Volts at 10 MHz

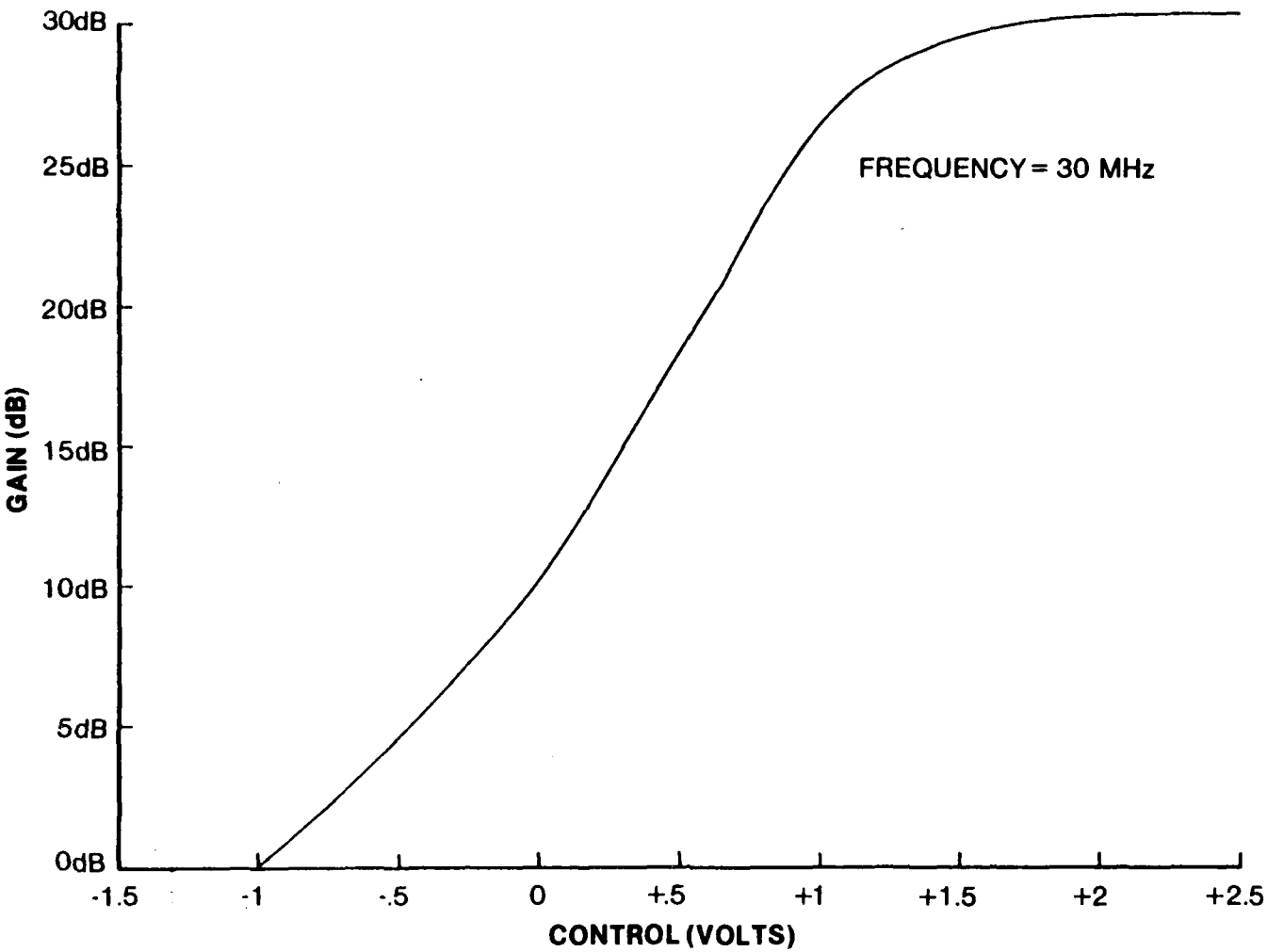



Figure 26. Variable Gain Amplifier Plot of Gain Versus Control Volts at 30 MHz

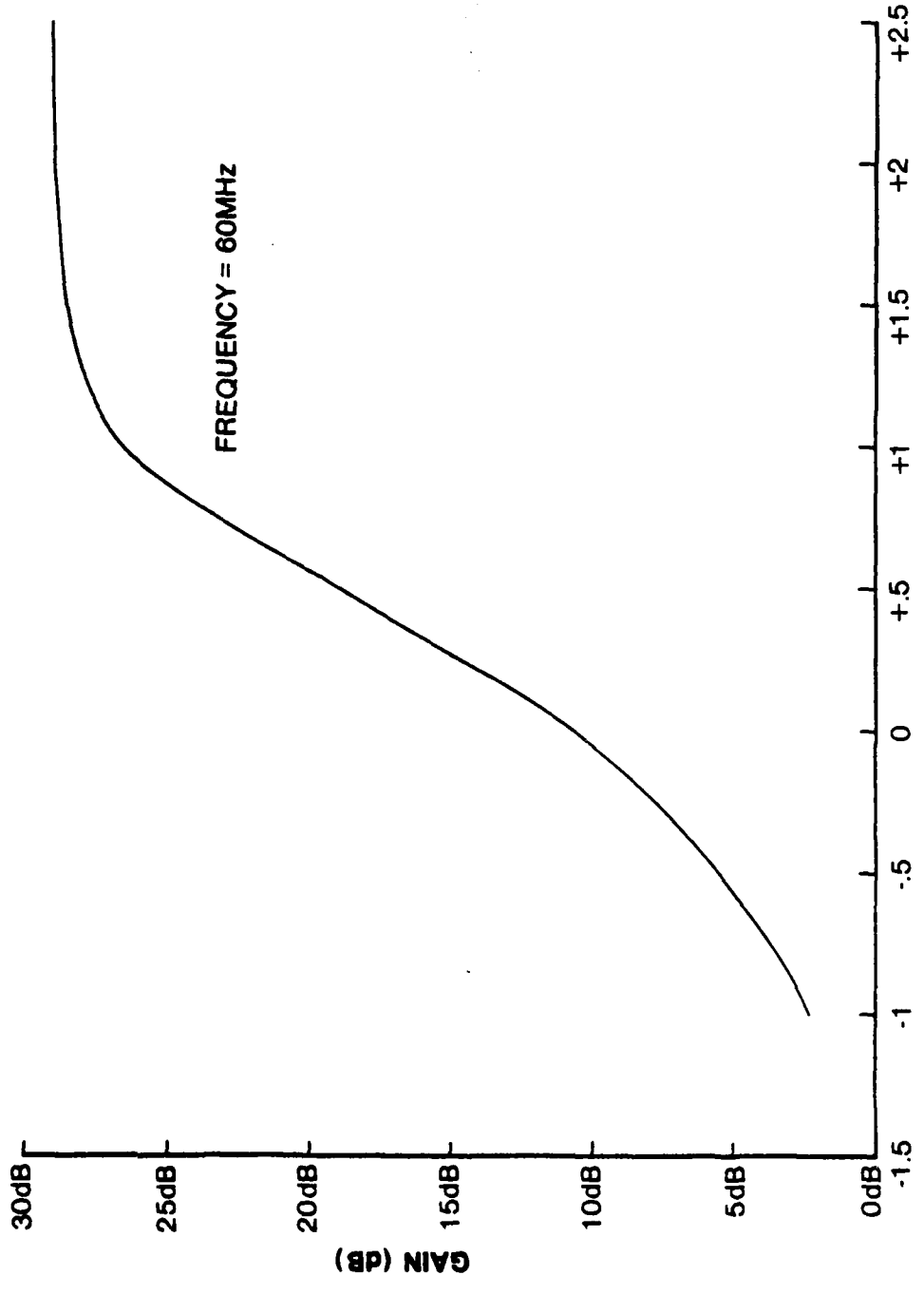



Figure 27. Variable Gain Amplifier Plot of Gain Versus Control Volts at 60 MHz

TABLE 2

VARIABLE GAIN AMPLIFIER EVALUATION DATA

| Input Power (dBm) | -12 | -22 | -32 | -42 | -52 | -62 | -72 | -82 | -92 | -100 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | RESULTANT OUTPUT POWER (dBm) | | | | | |
| Frequency (MHz) | | | | | | | | | | |
| .5 | 16.4 | 8.8 | -1.2 | -11.4 | -21.6 | -31.6 | -41.6 | -51.6 | -60.8 | -67.0 |
| 10.0 | 16.4 | 8.8 | -1.2 | -11.4 | -21.6 | -31.6 | -41.6 | -51.6 | -60.8 | -67.0 |
| 15.0 | 16.4 | 8.8 | -1.2 | -11.4 | -21.6 | -31.6 | -41.6 | -51.6 | -60.8 | -67.0 |
| 20.0 | 16.2 | 8.8 | -1.2 | -11.4 | -21.6 | -31.6 | -41.6 | -51.6 | -60.8 | -67.0 |
| 25.0 | 15.6 | 8.8 | -1.2 | -11.4 | -21.6 | -31.6 | -41.6 | -51.6 | -60.8 | -67.4 |
| 30.0 | 14.4 | 8.8 | -1.2 | -11.4 | -21.6 | -31.6 | -41.6 | -51.6 | -60.8 | -67.6 |
| 35.0 | 13.0 | 8.7 | -1.3 | -11.4 | -21.7 | -31.7 | -41.7 | -51.7 | -60.9 | -67.7 |
| 40.0 | 11.6 | 8.6 | -1.4 | -11.5 | -21.8 | -31.8 | -41.8 | -51.7 | -61.0 | -67.7 |
| 45.0 | 10.4 | 8.4 | -1.5 | -11.6 | -21.9 | -32.0 | -41.9 | -51.8 | -61.0 | -67.8 |
| 50.0 | 9.6 | 8.0 | -1.6 | -11.8 | -22.0 | -32.1 | -42.0 | -51.9 | -61.6 | -67.8 |
| 55.0 | 9.0 | 7.6 | -2.0 | -12.2 | -22.1 | -32.1 | -42.2 | -51.9 | -61.6 | -67.8 |
| 60.0 | 8.6 | 7.0 | -2.4 | -12.4 | -22.4 | -32.4 | -42.4 | -52.0 | -61.6 | -68.0 |
| 65.0 | 8.4 | 6.4 | -2.8 | -13.0 | -23.0 | -32.6 | -42.6 | -52.2 | -61.8 | -68.2 |
| 70.0 | 7.8 | 5.6 | -3.6 | -13.8 | -23.6 | -33.0 | -43.0 | -52.8 | -62.0 | -68.8 |
| 75.0 | 7.4 | 5.0 | -4.2 | -14.2 | -24.4 | -33.8 | -43.6 | -53.4 | -62.4 | -69.6 |
| 80.0 | 7.0 | 4.0 | -5.0 | -15.0 | -25.0 | -34.8 | -44.6 | -54.4 | -63.2 | -70.4 |
| 85.0 | 6.6 | 3.4 | -5.6 | -15.8 | -25.8 | -35.8 | -45.6 | -55.4 | -64.2 | -71.4 |
| 90.0 | 6.0 | 2.6 | -6.2 | -16.4 | -26.4 | -36.8 | -47.0 | -56.6 | -65.6 | -72.4 |
| 95.0 | --- | 2.0 | -7.0 | -17.0 | -27.0 | -38.0 | -47.8 | -57.6 | -66.2 | -73.0 |
| 100.0 | --- | 1.6 | -7.6 | -17.6 | -27.6 | -38.6 | -48.4 | -58.0 | -66.6 | -73.0 |

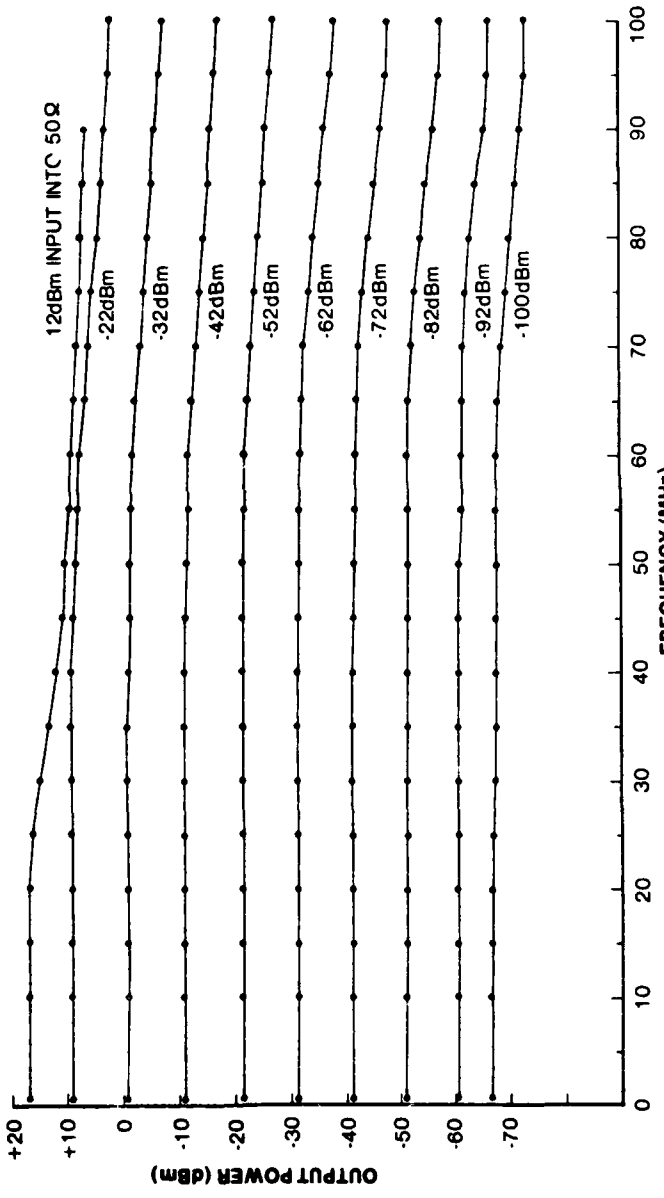



Figure 28. Variable Gain Amplifier Evaluation Plot of Output Power Versus Frequency

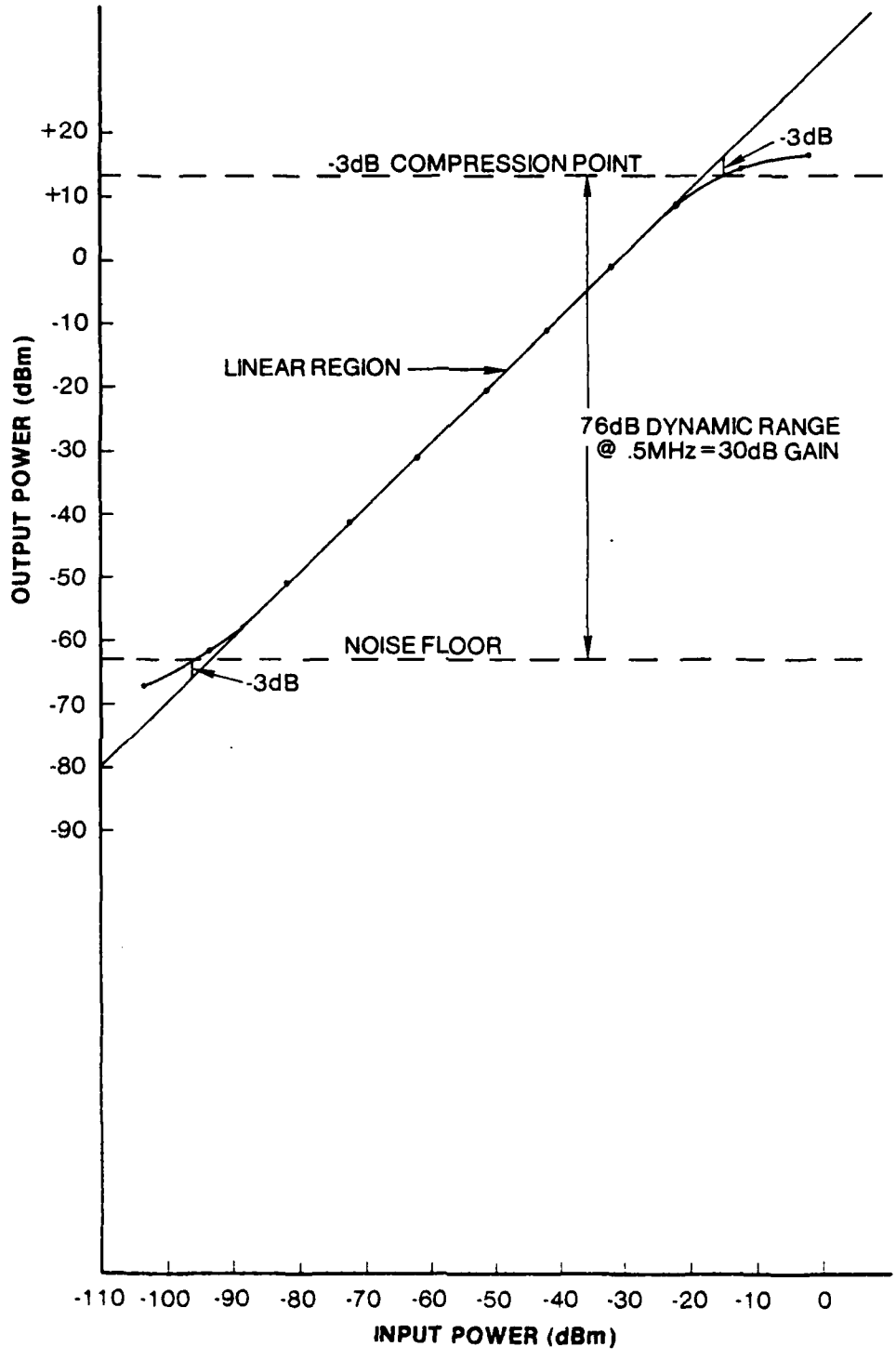



Figure 29. Variable Gain Amplifier Evaluation Plot of Output Power Versus Input Power at .5 MHz

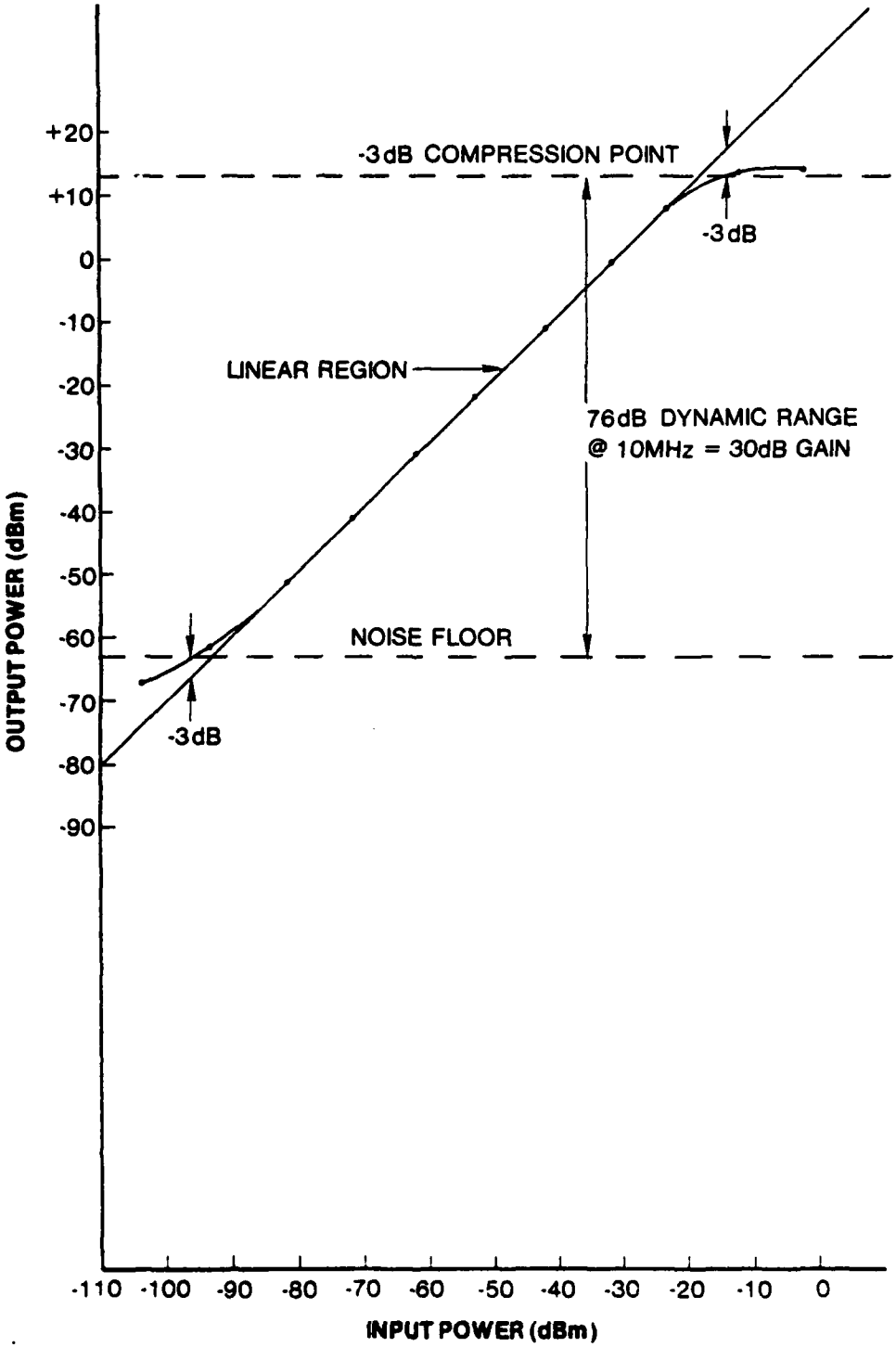



Figure 30. Variable Gain Amplifier Evaluation Plot of Output Power Versus Input Power at 10 MHz

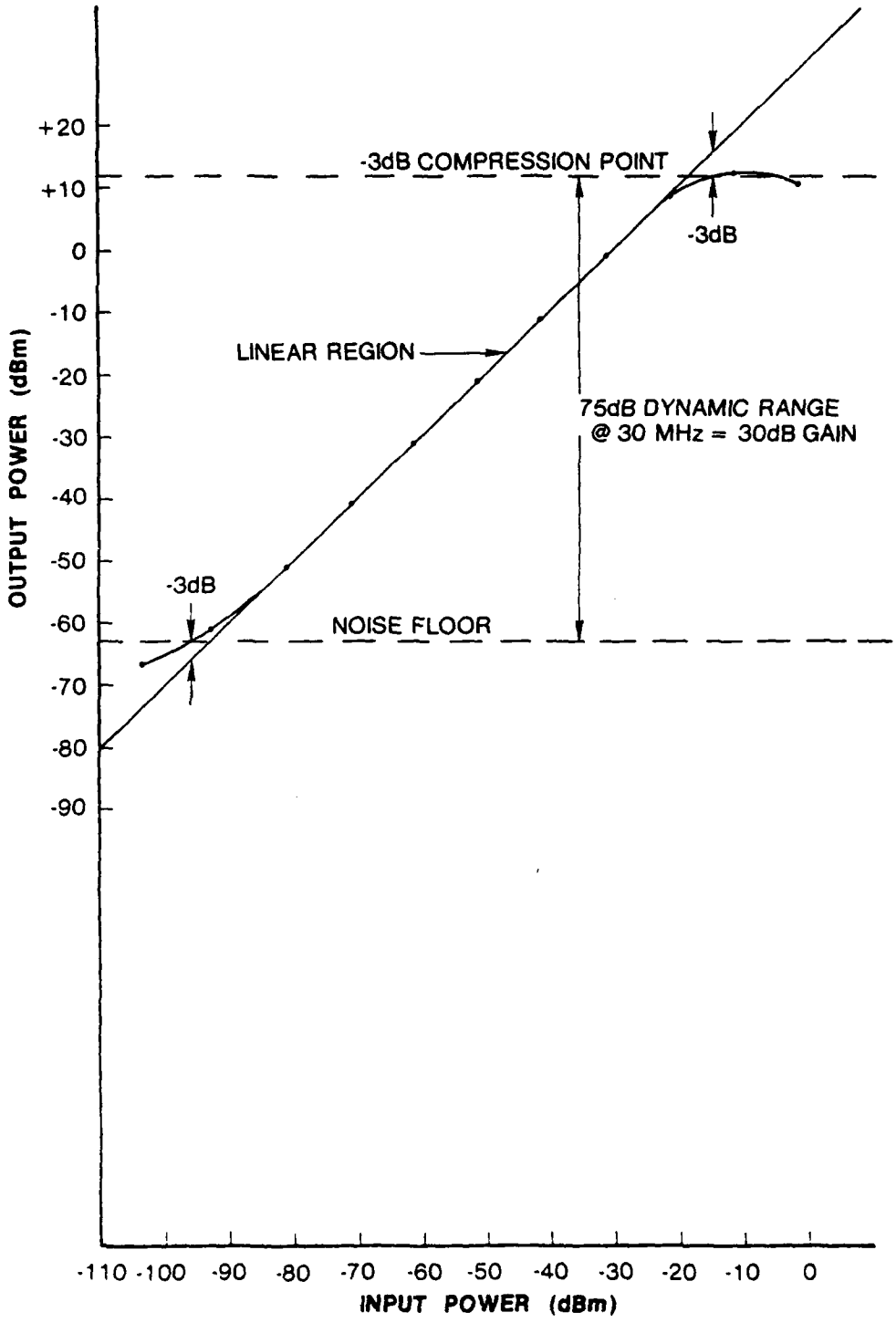



Figure 31. Variable Gain Amplifier Evaluation Plot of Output Power Versus Input Power at 30 MHz

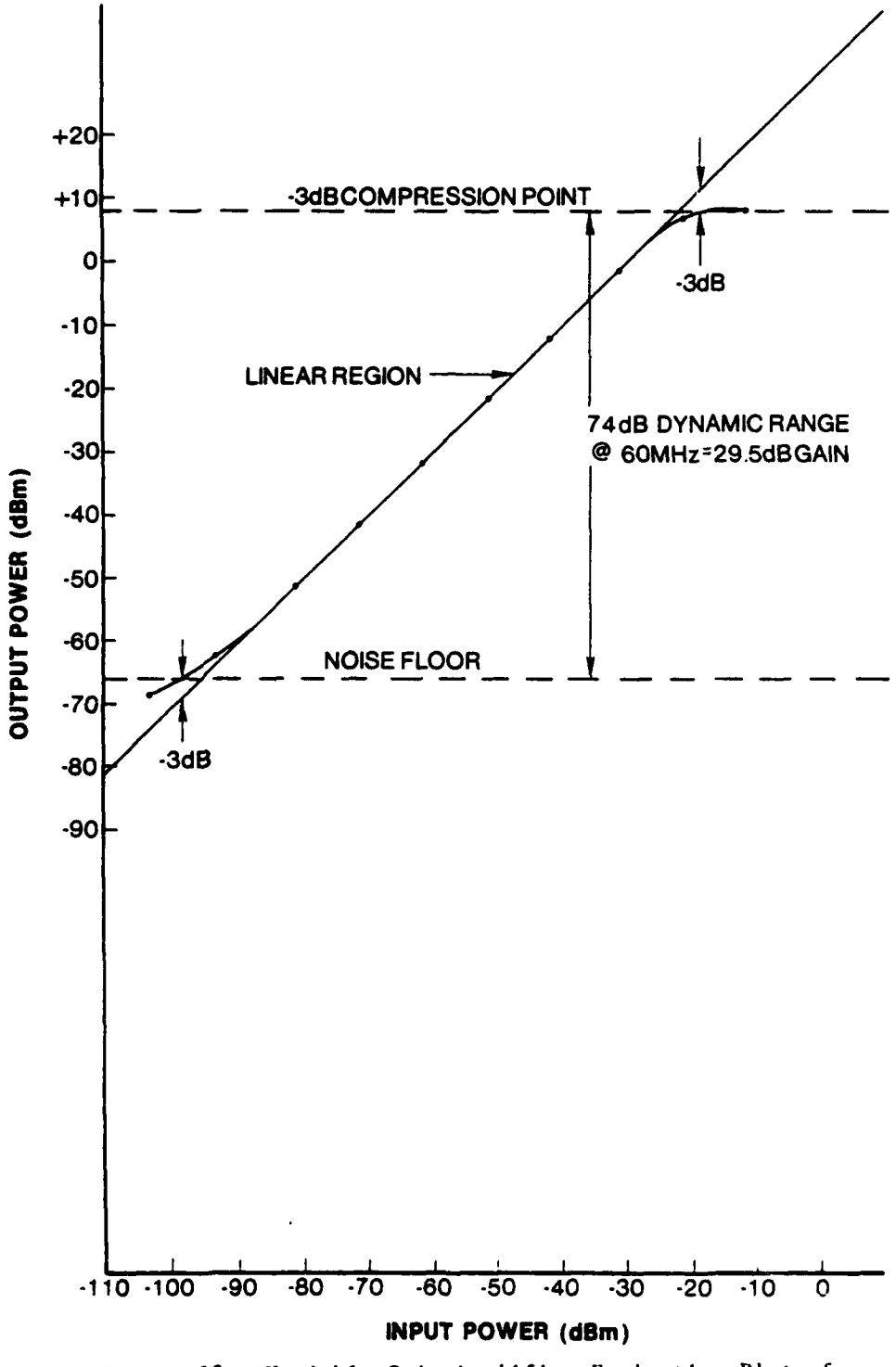



Figure 32. Variable Gain Amplifier Evaluation Plot of Output Power Versus Input Power at 60 MHz

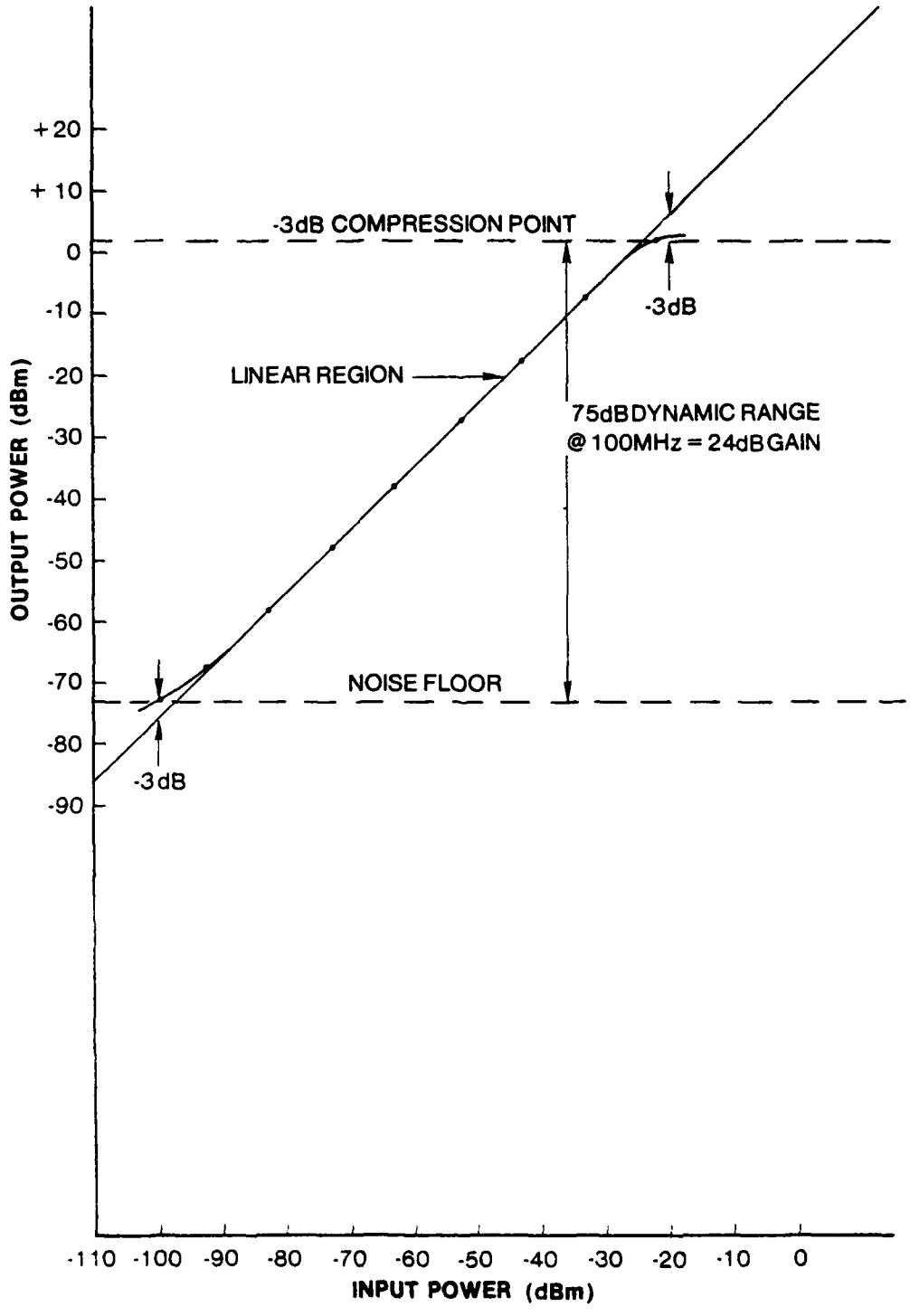



Figure 33. Variable Gain Amplifier Evaluation Plot of Output Power Versus Input Power at 100 MHz

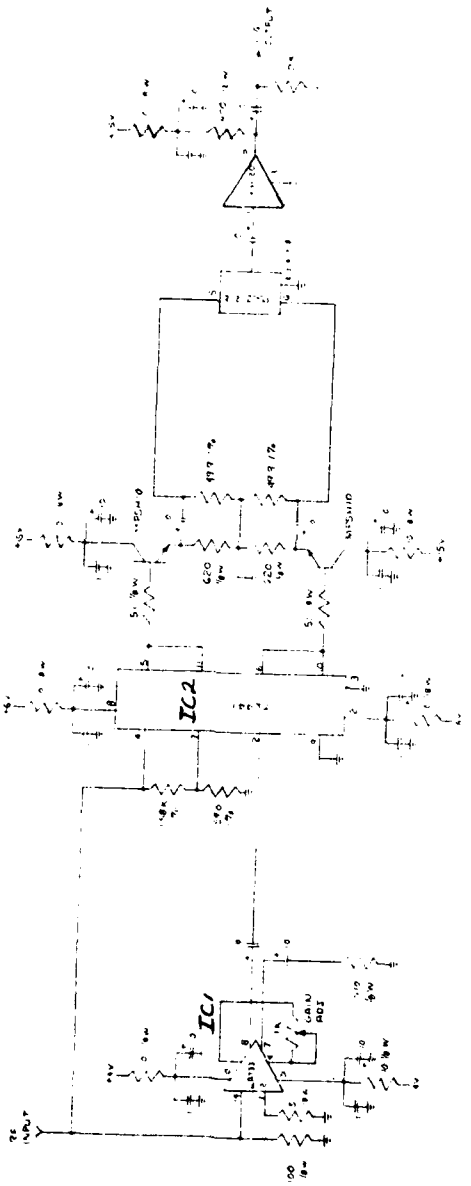



Figure 34. Logarithmic Amplifier Schematic

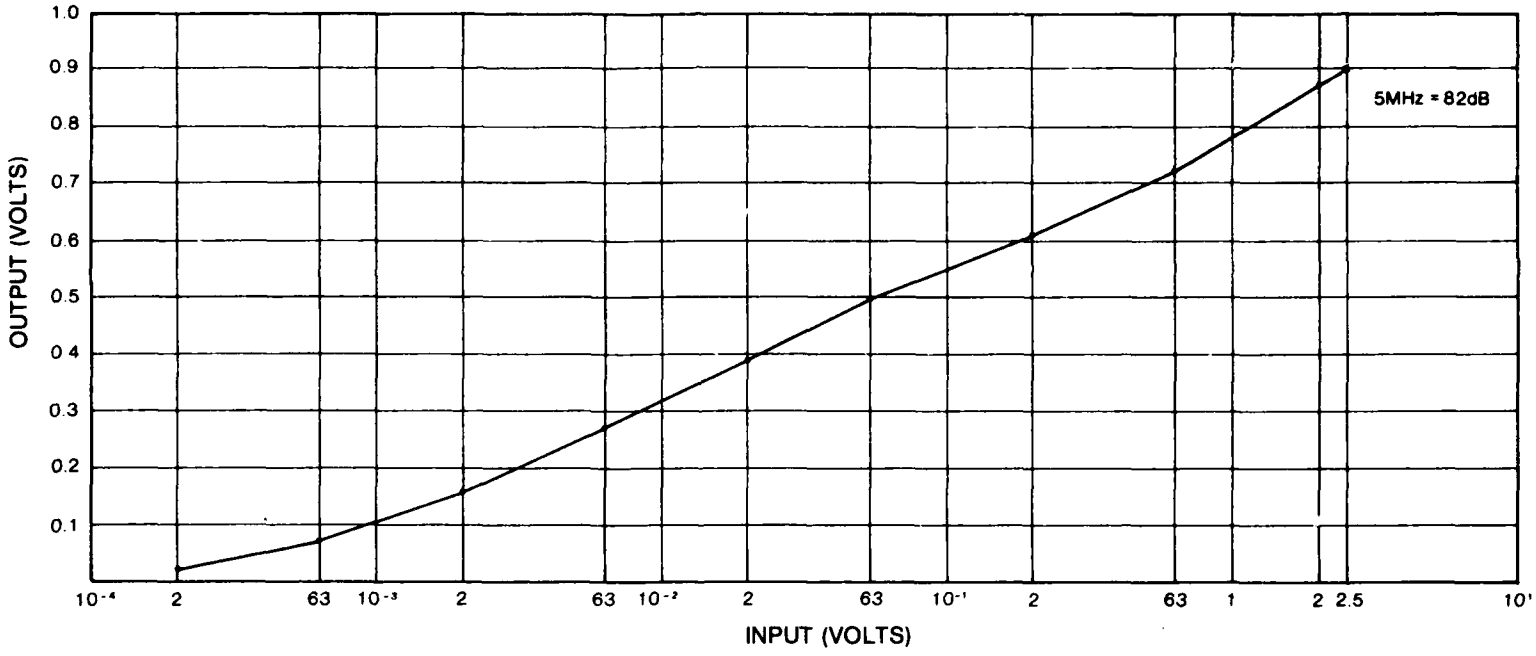



Figure 35. Logarithmic Amplifier Evaluation Plot of Input Volts Versus Output Volts at 5 MHz

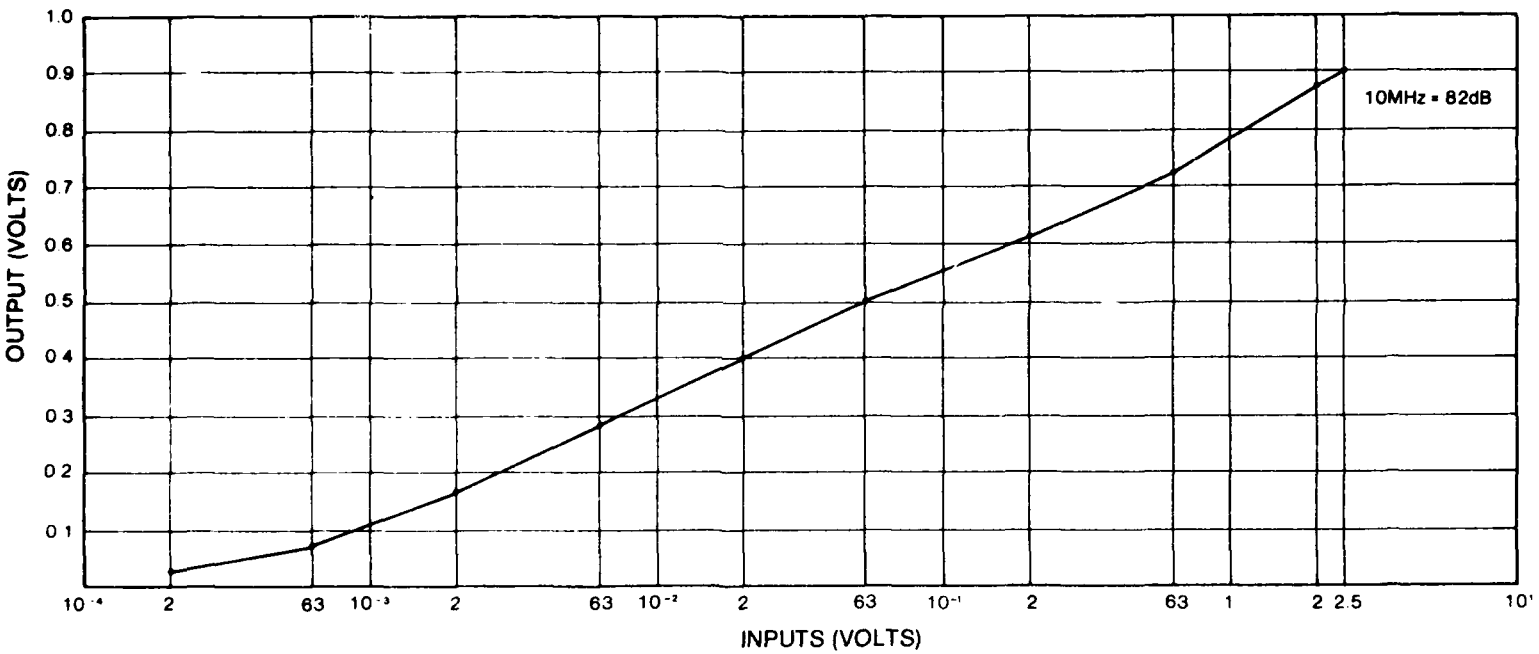



Figure 36. Logarithmic Amplifier Evaluation Plot of Input Volts Versus Output Volts at 10 MHz

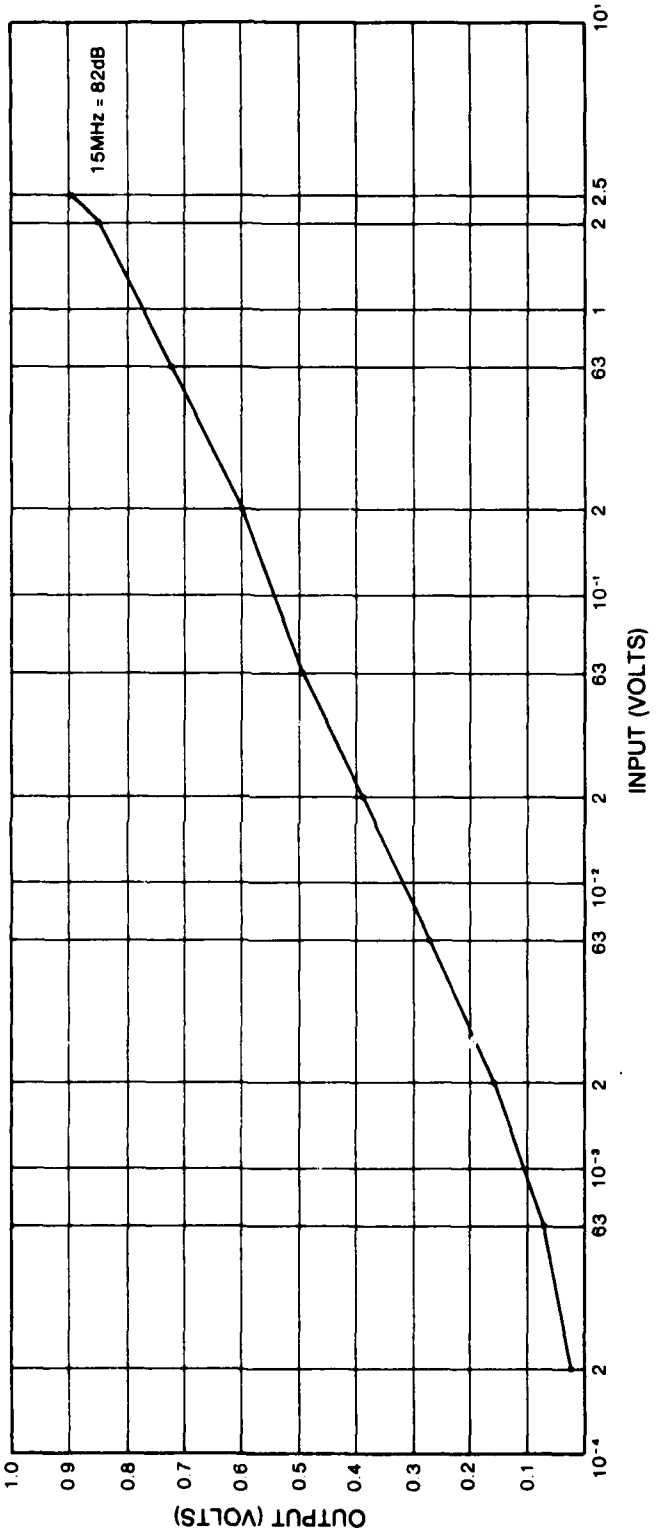



Figure 37. Logarithmic Amplifier Evaluation Plot of Input Volts Versus Output Volts at 15 MHz

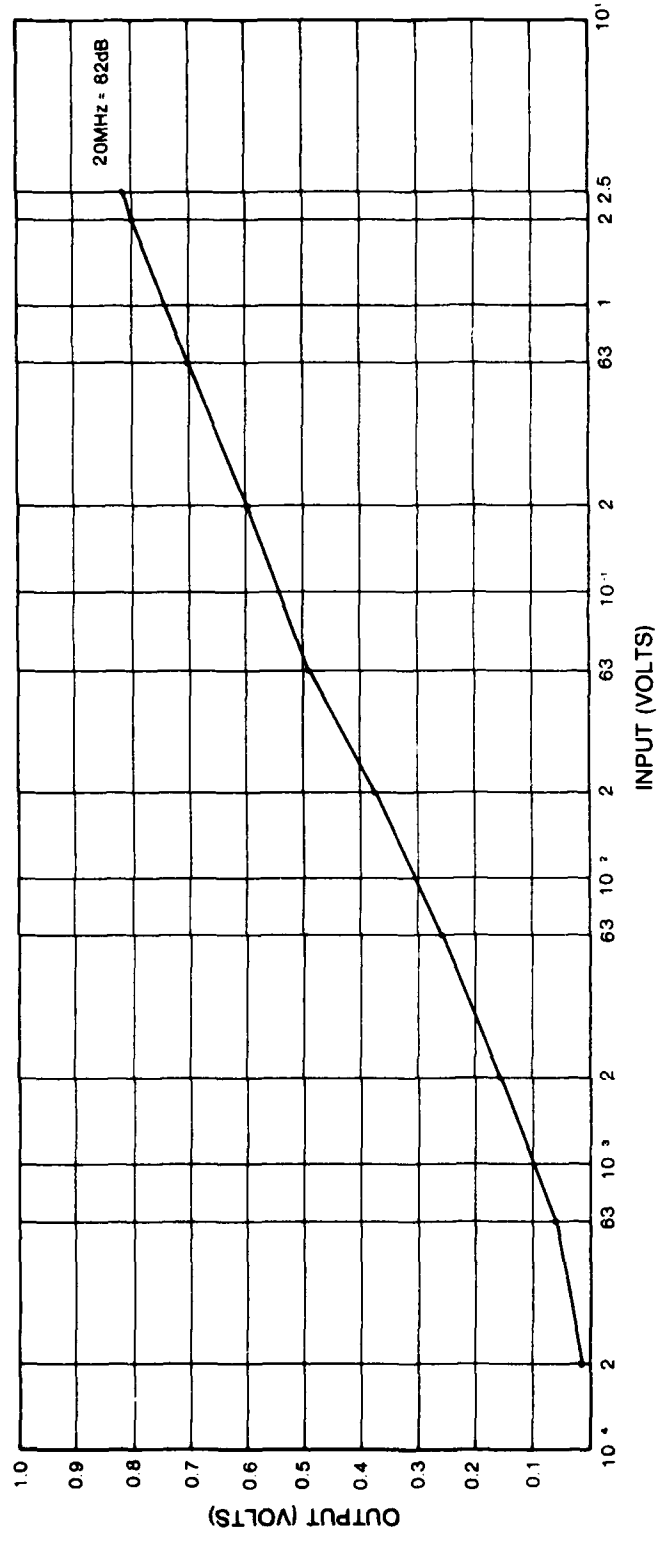



Figure 38. Logarithmic Amplifier Evaluation Plot of Input Volts Versus Output Volts at 20 MHz

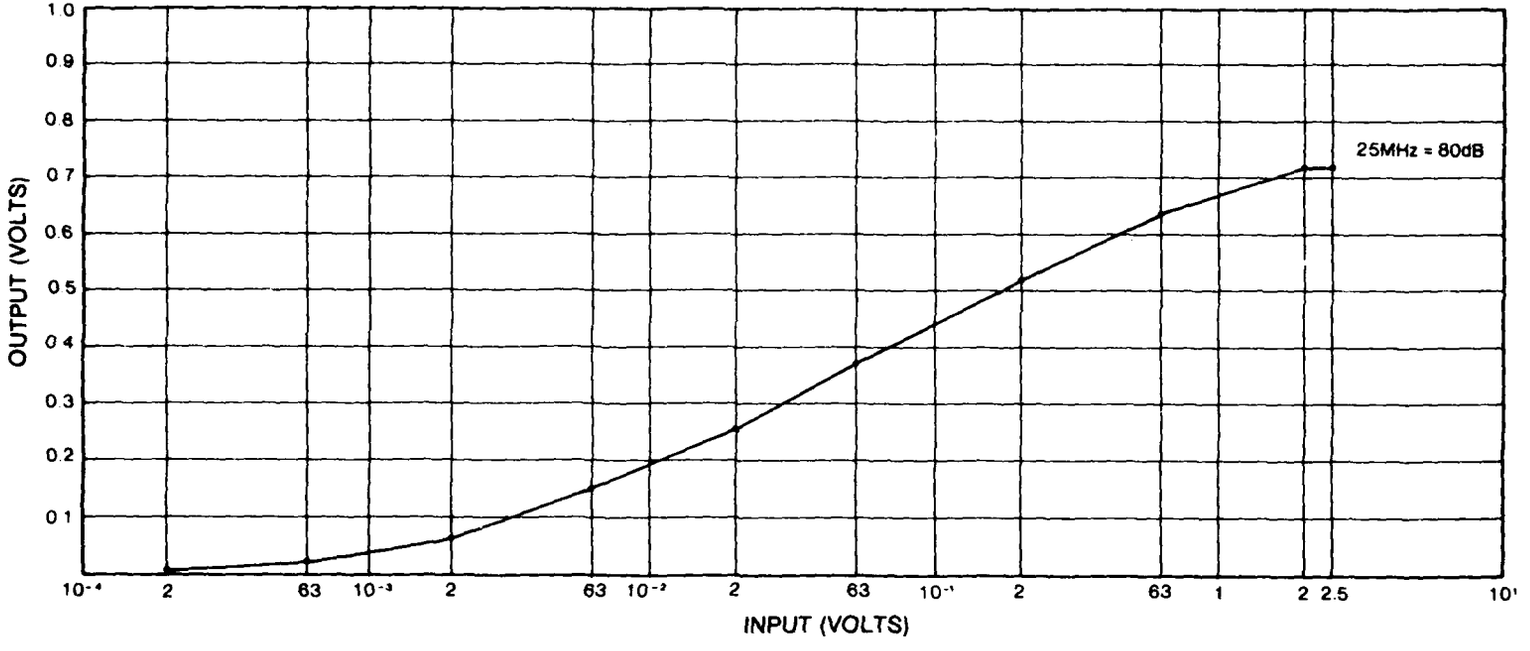



Figure 39. Logarithmic Amplifier Evaluation Plot of Input Volts Versus Output Volts at 25 MHz

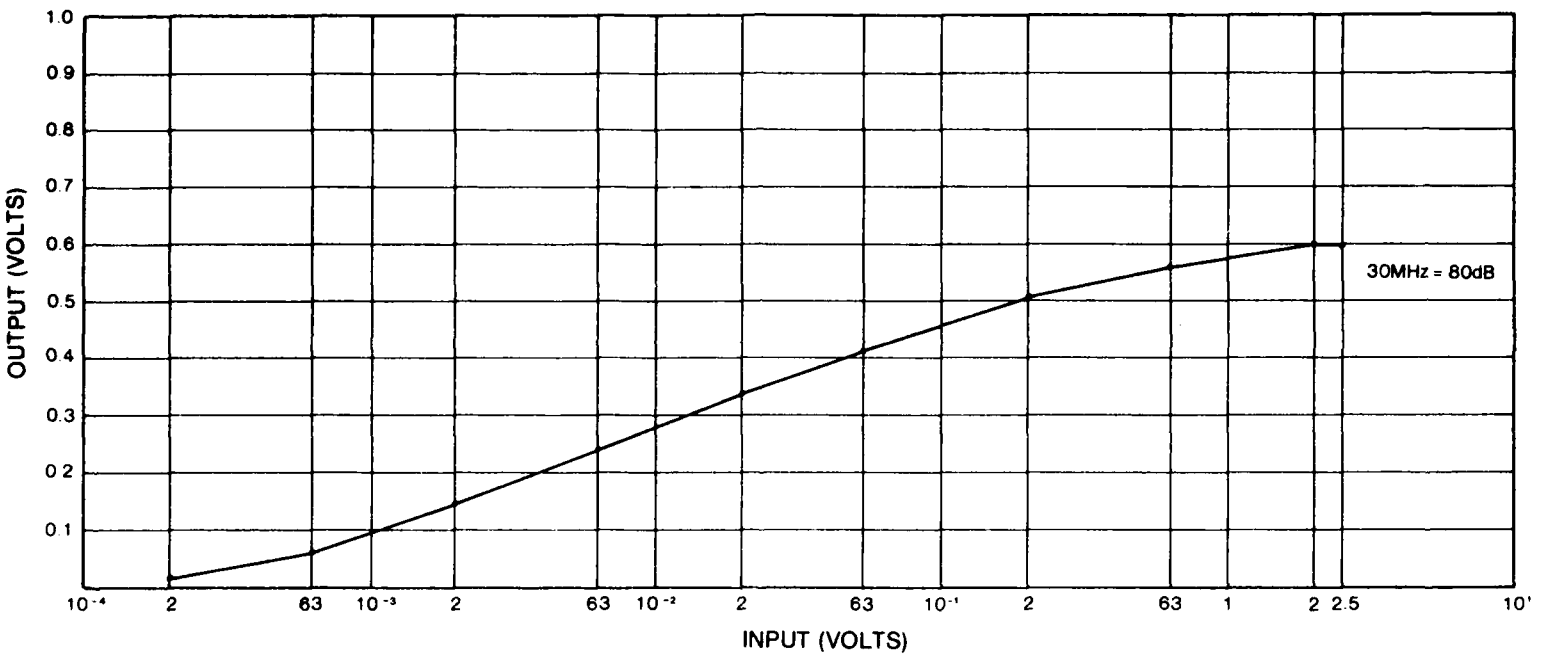



Figure 40. Logarithmic Amplifier Evaluation Plot of Input Volts Versus Output Volts at 30 MHz

## 10. RECEIVER FILTER

The schematic for the receiver filter design is shown in Figure 41. The design includes ten high pass filters and two sharp cutoff low pass filter options. The sharp cutoff low pass filters were selected to reduce the effects of sampling errors when the output RF signal is digitized.

The high pass filters are selected by the selection of relays K1 through K4. The relays are selected in combination to achieve the ten cutoff frequencies.

The relays K5 through K10 are used to select the three low pass filter positions. The 10 MHz filter is selected by the combination of K9 and K10. The 25 MHz filter is selected by K5 and K6, and the 85 MHz filter is selected by K7 and K8. All relays used for the high and low pass filters are TTL compatible and switch by applying a logic high level to pin 3.

The filter section also contains two attenuators for gain control. The attenuators are selected by relays K11 and K12 and are part of the overall gain control chain.

## 11. OUTPUT AMPLIFIER

The schematic for the output amplifier is shown in Figure 42. The amplifier's gain is approximately +12 dB and will drive a 50 ohm load to 5 volts peak-to-peak over the entire 85 MHz bandwidth. The amplifier was tested using a 50 foot coaxial cable terminated into a 50 ohm load. It was found that the degradation to the frequency response was negligible.

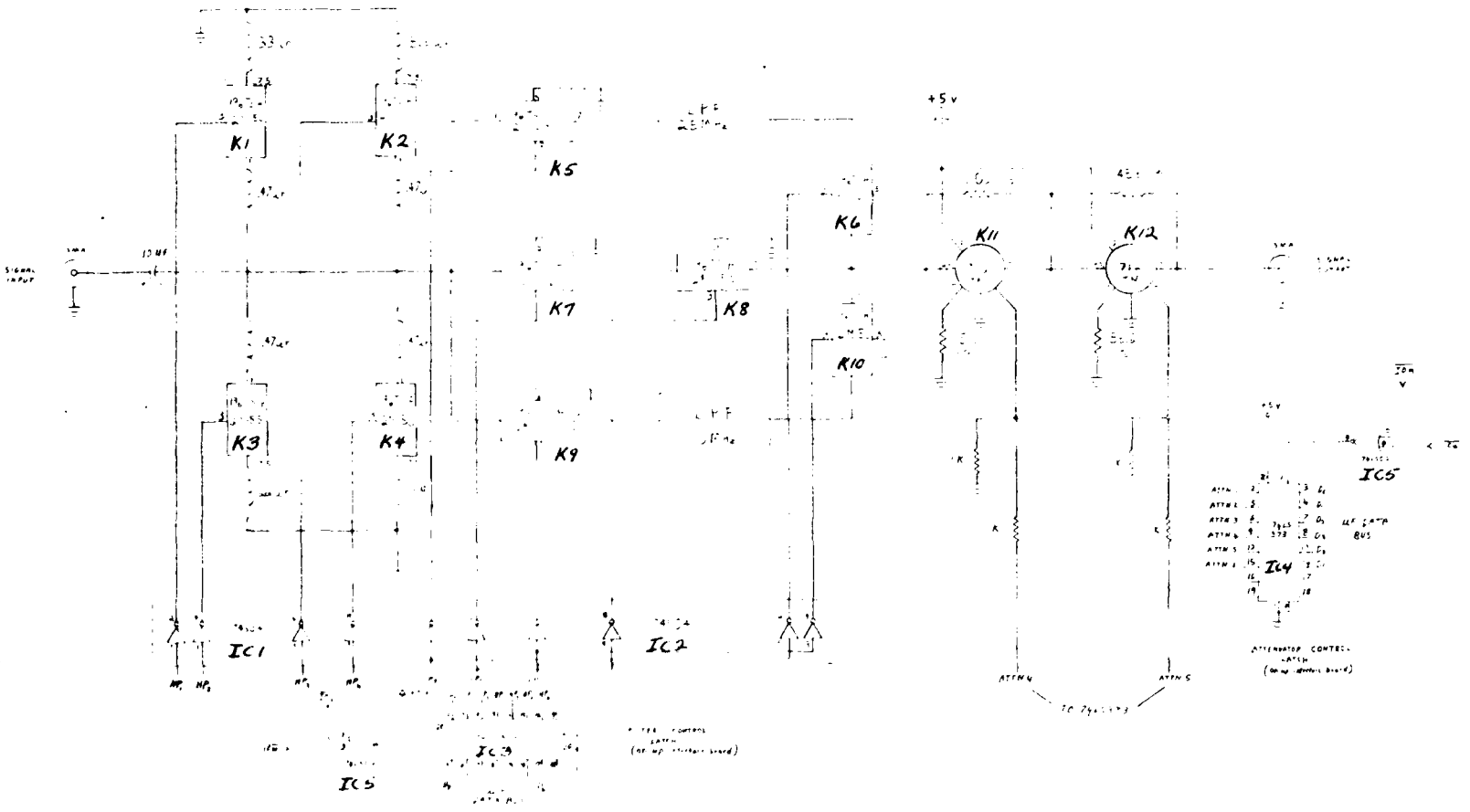



Figure 41. Receiver Filter Schematic

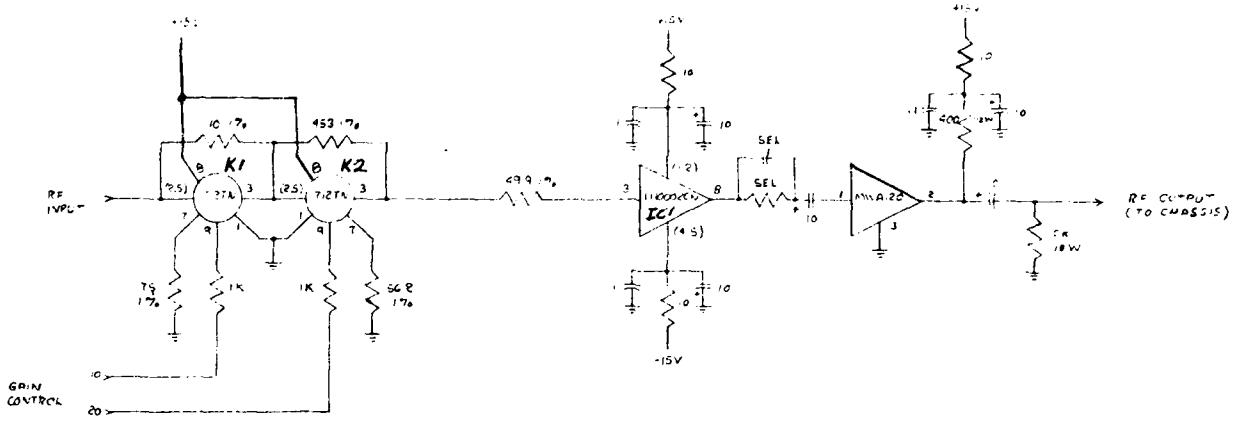



Figure 42. Output Amplifier Schematic

## 12. PULSER SWITCH

The schematic for the pulser switch is shown in Figure 43. The circuit was designed to discharge the output series capacitor once the capacitor has been fully charged to the high voltage supply output. The rate of discharge primarily determines the fall time of the output pulse. The output pulse fall time has been measured to be 5 to 8 nanoseconds depending on the high voltage supply output.

The fast discharge rate is achieved by the stacking of high speed, silicon-controlled rectifiers (SCR). The SCR's are biased in the avalanche mode rather than the switch mode. The trigger is applied to the first SCR. The three relays, K1, K2, and K3, as shown in the schematic, short out sections of the SCR stack when programmed to do so by the microprocessor system. The relays insure that the pulser switch maintains the avalanche mode when the pulser supply is adjusted to a lower voltage.

## 13. PULSER TUNING

The pulser tuning control provides for the broad range selection of inductive ($X_L$) and capacitive ($X_C$) elements used in the tuning network. The pulser tuning circuit schematic is shown in Figure 44.

The inductive elements are selected by relays K1 through K10 and the capacitive elements are selected by relays K11 through K19. Each element selected will be in series with the pulser output. The relays are a high voltage type and are selected by pulling pin 13 low to ground. The VN10KM transistors are used to interface the TTL logic levels and the coils in the relays.

The evaluation of numerous transducers has shown that, for a specific transducer frequency, a single tuning arrangement will not produce optimum results for all transducers with the same specifications. The input to the transducer will appear capacitive to

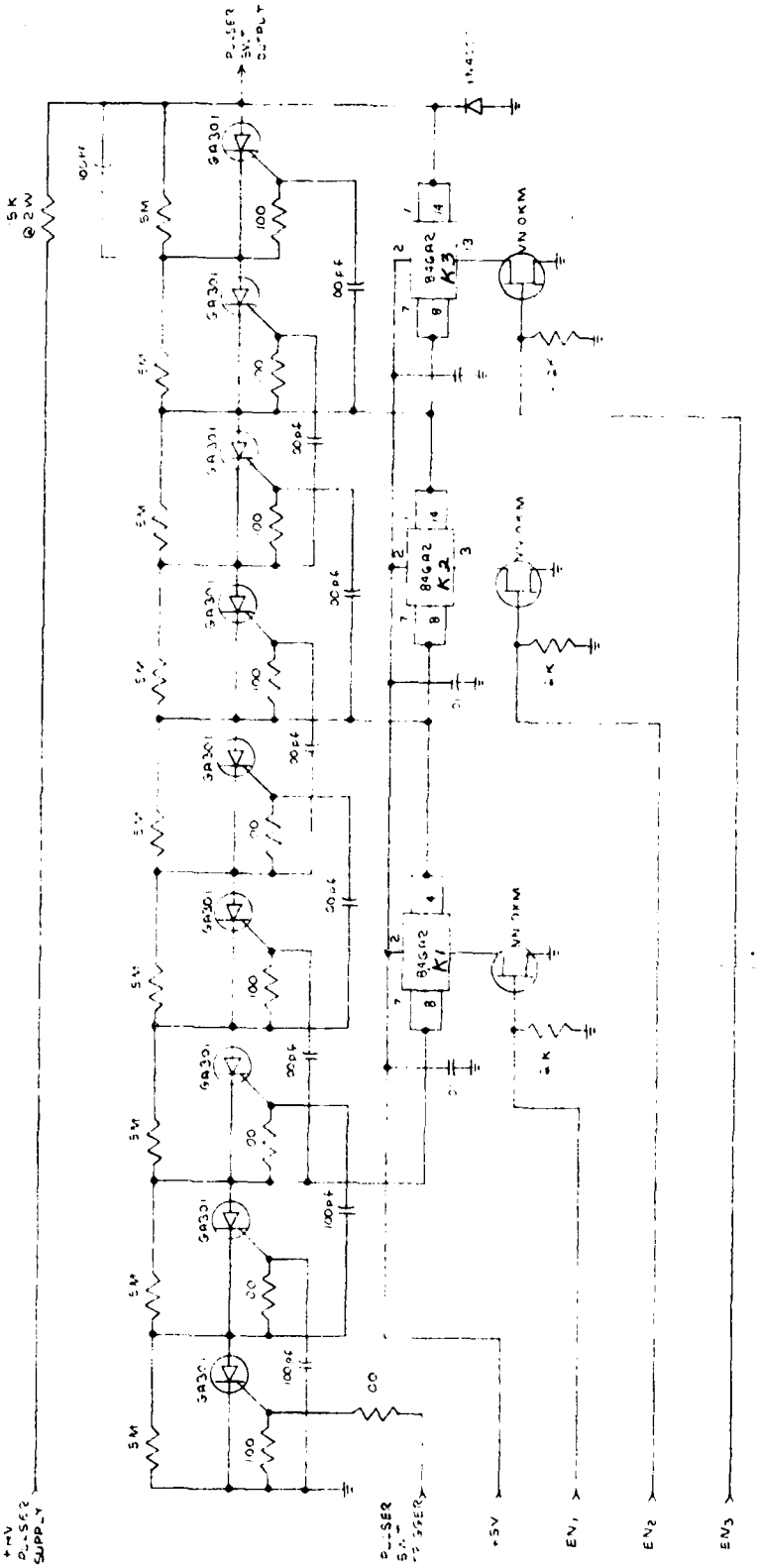



Figure 43. Pulser Switch Schematic

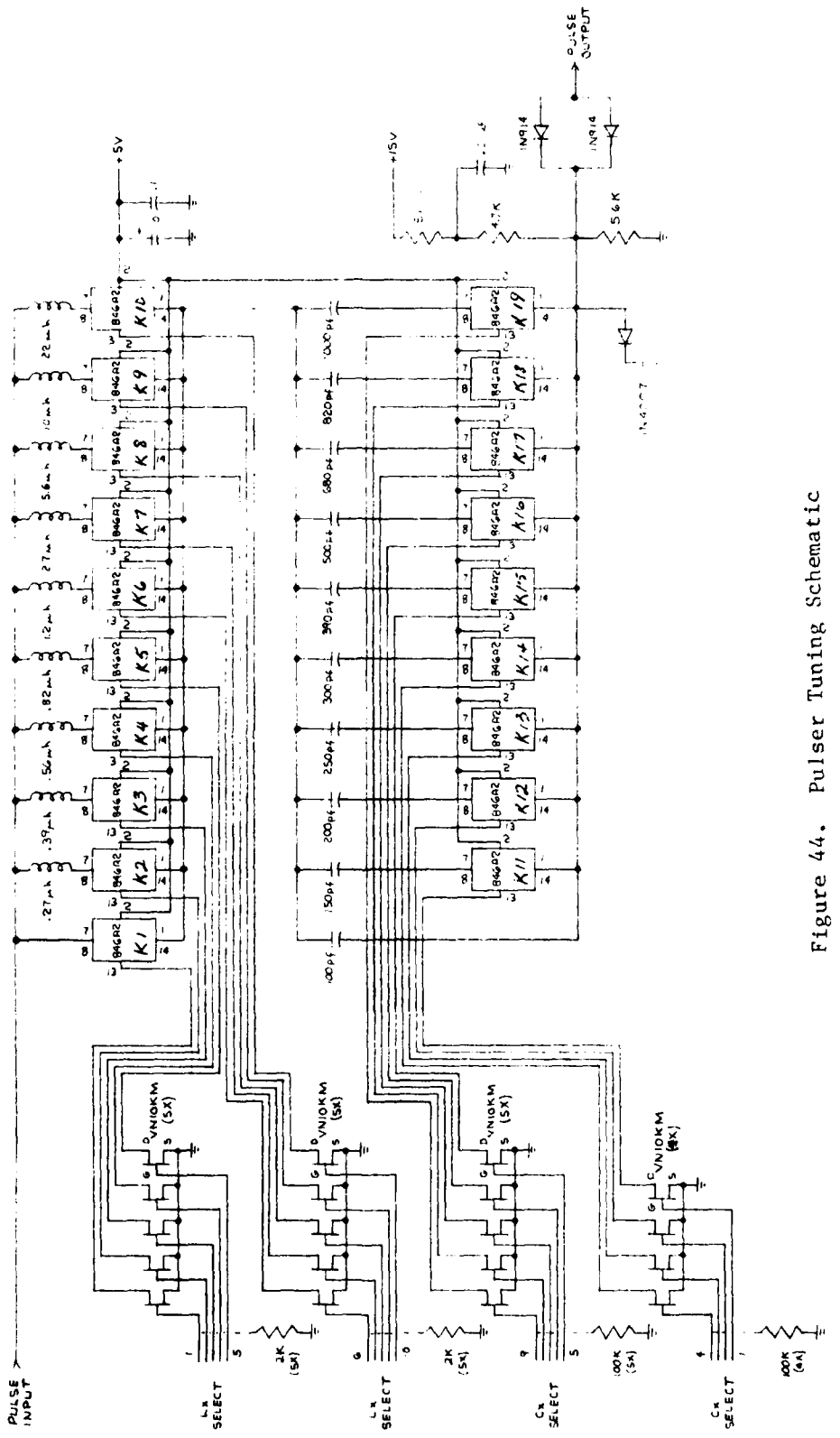



Figure 44. Pulser Tuning Schematic

inductive, depending on the construction and tuning of the transducer. The tuning circuit was designed to compensate for the transducer variations and allow for the maximum power transfer within the pass-band of the transducer. An increase in the range resolution of transducers tested, particularly at the higher frequencies, have been noted with the use of this tuning control.

The combination of $X_L$ and $X_C$ is selected by the front panel switch and read by the microprocessor. The selection of 100 different combinations of $X_L$ and $X_C$ are possible with this tuning circuit. The microprocessor interface schematic is shown in Figure 45. ICs 2, 3, and 4 are used as the data hold latches.

## 14. PULSER SUPPLY SWITCH

The schematic for the pulser supply switch is shown in Figure 46. The circuitry was designed as a high voltage switch between the high voltage supply and the pulser switch. The switch is turned off just before the pulser switch is triggered and is off long enough for the pulser switch to recover. The pulser supply switch is then turned on to charge the series output capacitor. The pulser supply switch provides for the reduction of output power requirement of the pulser supply and the increase in pulse repetition rate. The pulser trigger generator schematic is shown in Figure 47.

## 15. DAMPING CONTROL

The schematic for the damping control circuitry is shown in Figure 48. The circuitry provides for the remote selection of pulser output damping resistors. The damping can be selected from 10 ohms to 990 ohms in 10 ohm steps. The relays K1 through K10 select the 100 ohms position and the relays K11 through K20 select the 10 ohms position. These groups of relays are used in combination to achieve the 10 ohm steps. To select 620 ohms, for example, relays K4 and K19 will be activated. The damping is programmed by the microprocessor

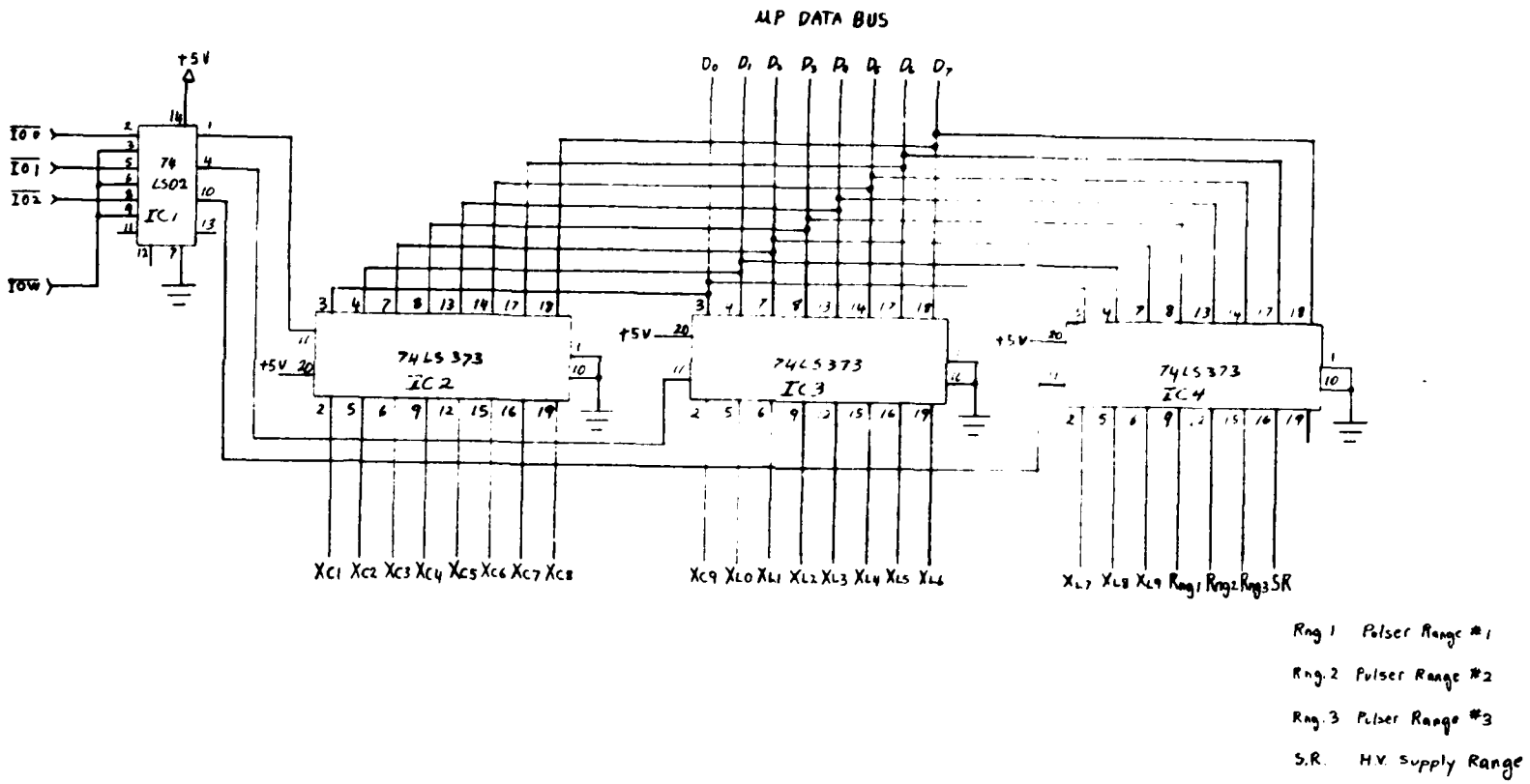



Figure 45. Pulser Tuning Interface Schematic

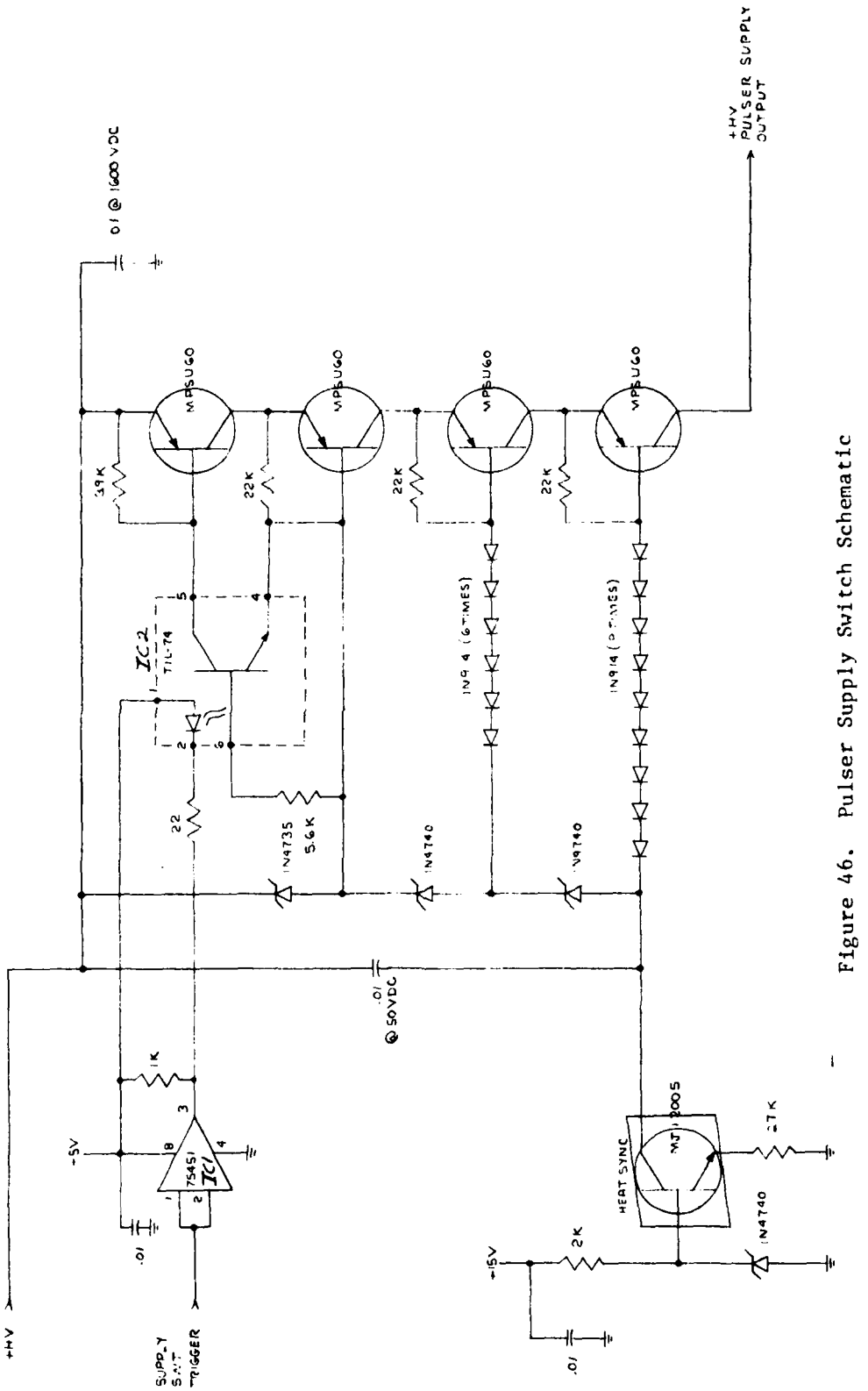



Figure 46. Pulser Supply Switch Schematic

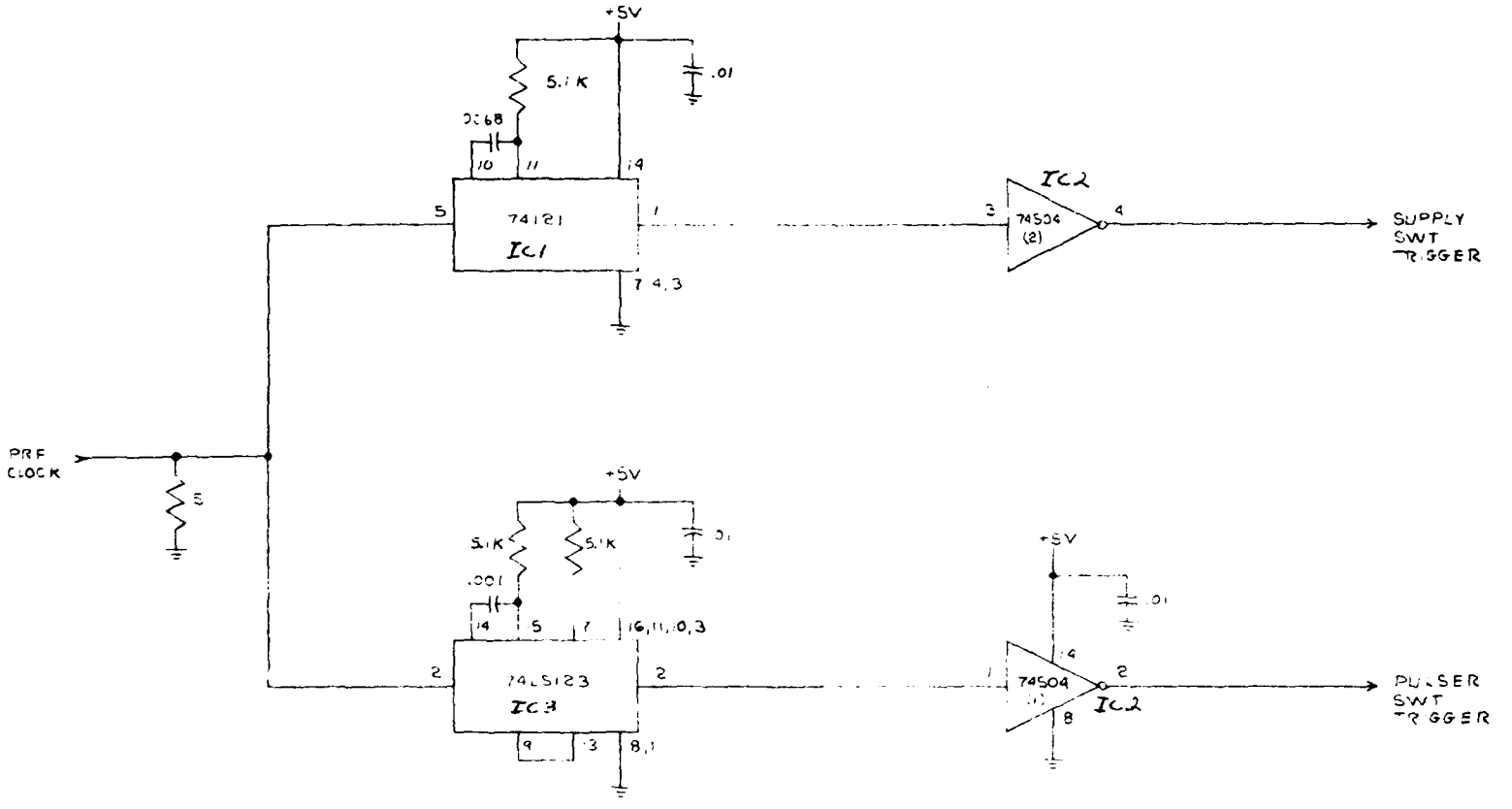



Figure 47. Pulser Trigger Generator Schematic

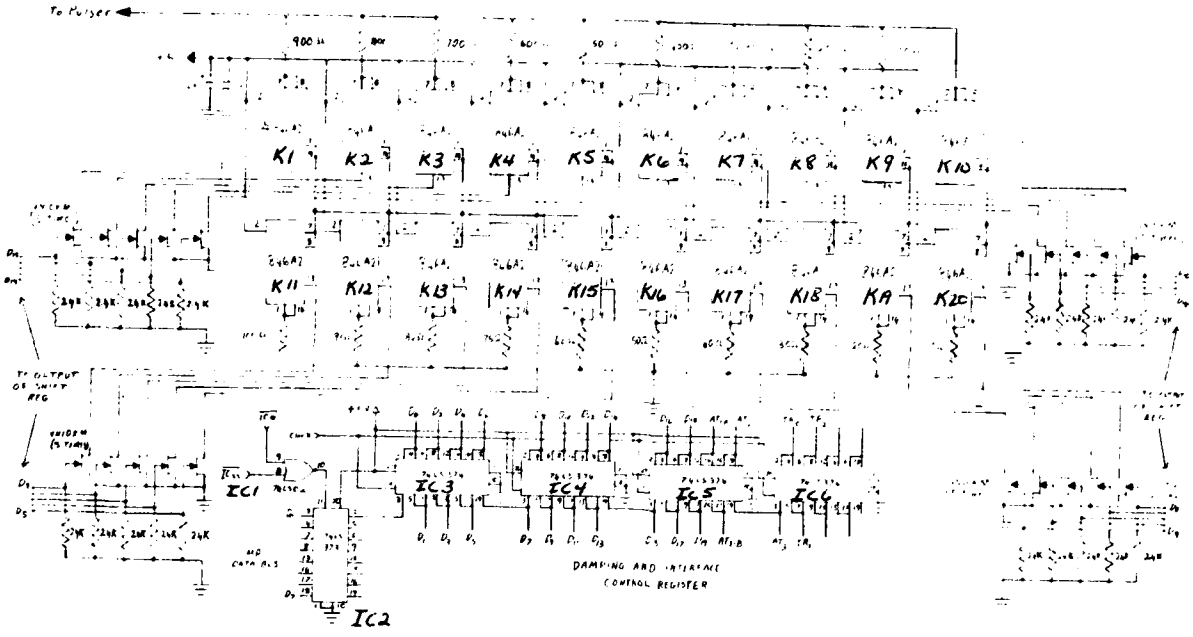



Figure 48. Damping Control Schematic

and selected via the front panel switches. ICs 3 through 6 are used as the data hold latches.

## 16. PULSER SUPPLY

The schematic for the pulser supply circuitry is shown in Figure 49. The circuitry develops the high voltages necessary to charge the series output pulser capacitor. The maximum output is 1200 volts at 20 milliamps, 24 watts. The pulser supply output voltage is controlled by the microprocessor. The circuitry shown in Figure 50 converts the digital codes to analog, for the pulser supply input control. The digital binary codes to control the output of the pulser supply are converted to analog levels by the digital-to-analog converter, IC 6. The interface amplifier, IC 7, scales the output of the digital-to-analog converter to control the pulser supply over the full range.

The digital codes, which correspond to a selected pulser volts output, are stored in the microprocessor memory system. The codes were preselected to produce an approximate pulser output amplitude. The pulser output amplitude will vary depending on the damping and tuning positions selected and the transducer load requirements.

A software, closed loop, control algorithm was developed to monitor the pulser output amplitude and adjust the pulser supply, to compensate for the output amplitude changes due to various load conditions. The algorithm produced a low frequency oscillation (hunting) affect on the pulser output amplitude. The control algorithm was not sufficiently corrected and, therefore, was not incorporated as a software function.

## 17. PULSER OUTPUT MEASUREMENT AND CONTROL

The schematic of the pulser output measurement and control is shown in Figure 50. The circuitry provides for the analog-to-digital

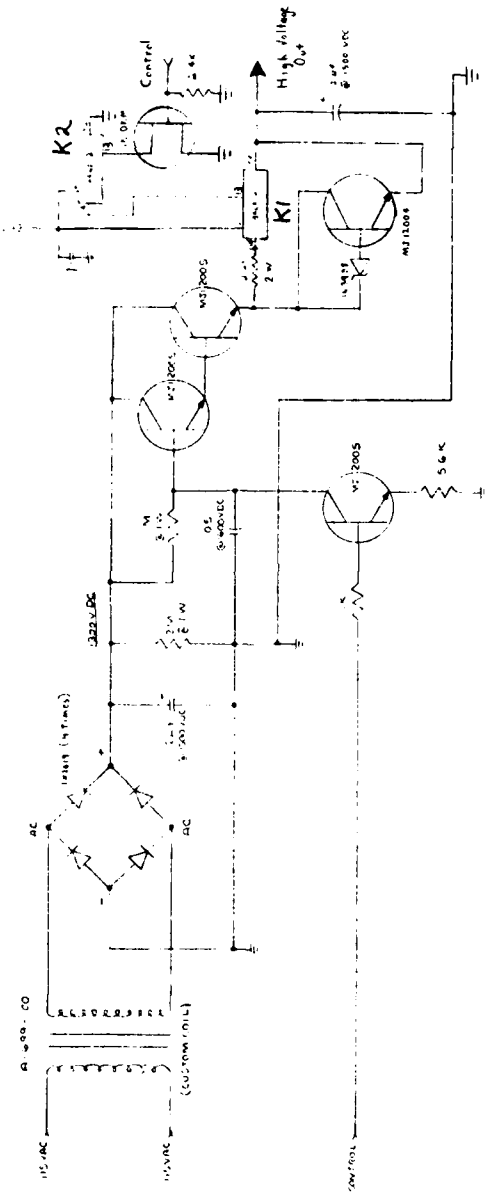



Figure 49. Pulser Supply Schematic

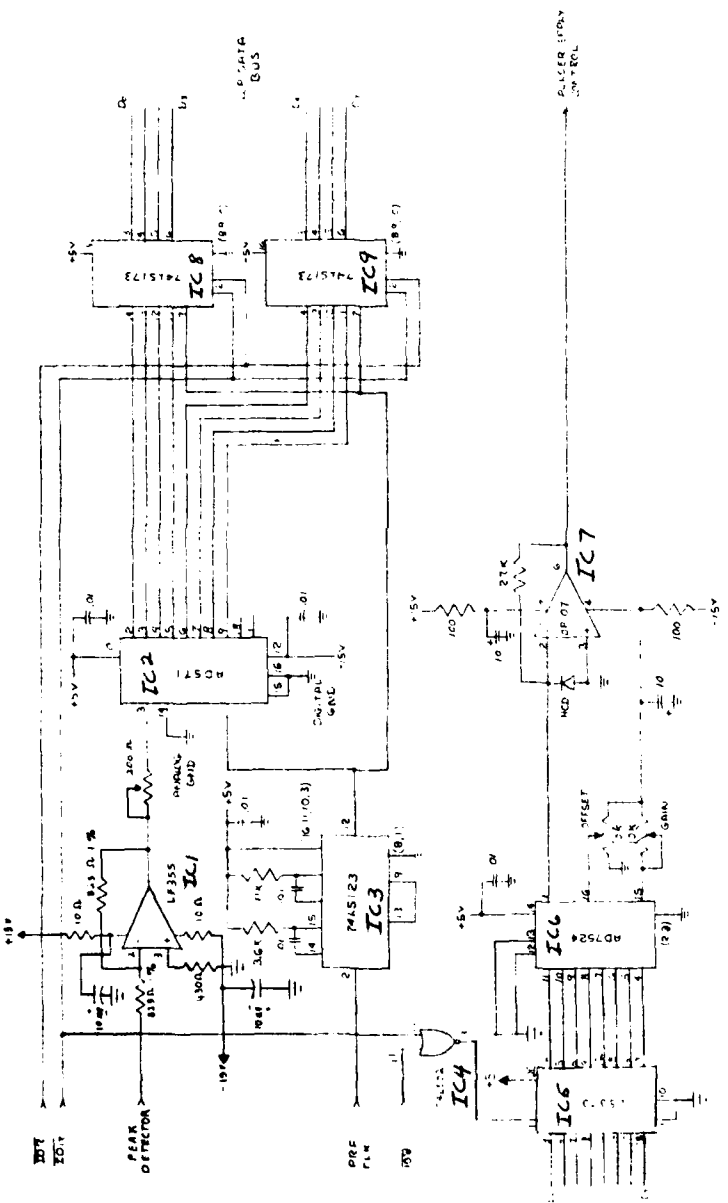



Figure 50. Pulser Output Measurement and Control Schematic

conversion of the peak detected pulser output and the digital-to-analog conversion for the pulser supply control. The pulser output is monitored by the microprocessor each pulse repetition.

The output of the pulser peak detector is connected to the input of the inverting buffer amplifier, IC 1. The output of the buffer is converted to binary codes by the analog-to-digital converter, IC 2. The conversion codes are stored in the latches, IC 8 and IC 9 and read by the microprocessor.

## 18. AMPLIFIER INTERFACE

The schematic for the amplifier interface is shown in Figure 51. The circuitry provides for the interface between the pulser output and the RF linear and logarithmic amplifiers and the selection of pulse-echo mode (T/R), pitch-catch mode (T→R), receive-only mode (R), the high-isolation mode (OFF), the front-end attenuators, and the pulser output peak detector. The circuitry is controlled by the microprocessor.

The pulser peak detector is shown at the top of the schematic. The pulser output is scaled down, by a factor of 100, at the input to the detector section. The input buffer transistor is used to drive the diode and capacitor in the actual peak detection section. The buffer amplifier, IC 3, isolates the peak detector elements and the output. The peak detector is reset at the beginning of each pulser cycle. Testing has shown the detector to underestimate the actual peak value at the pulser's output.

The transducer mode select is determined by the relays K1 through K5. In this "T/R" mode, relays K1, K4, and K5 are selected. The pulser output is not connected to the receiver (R) input in this mode. The relays K1, K2, and K3 are selected when operating in the "T→R"

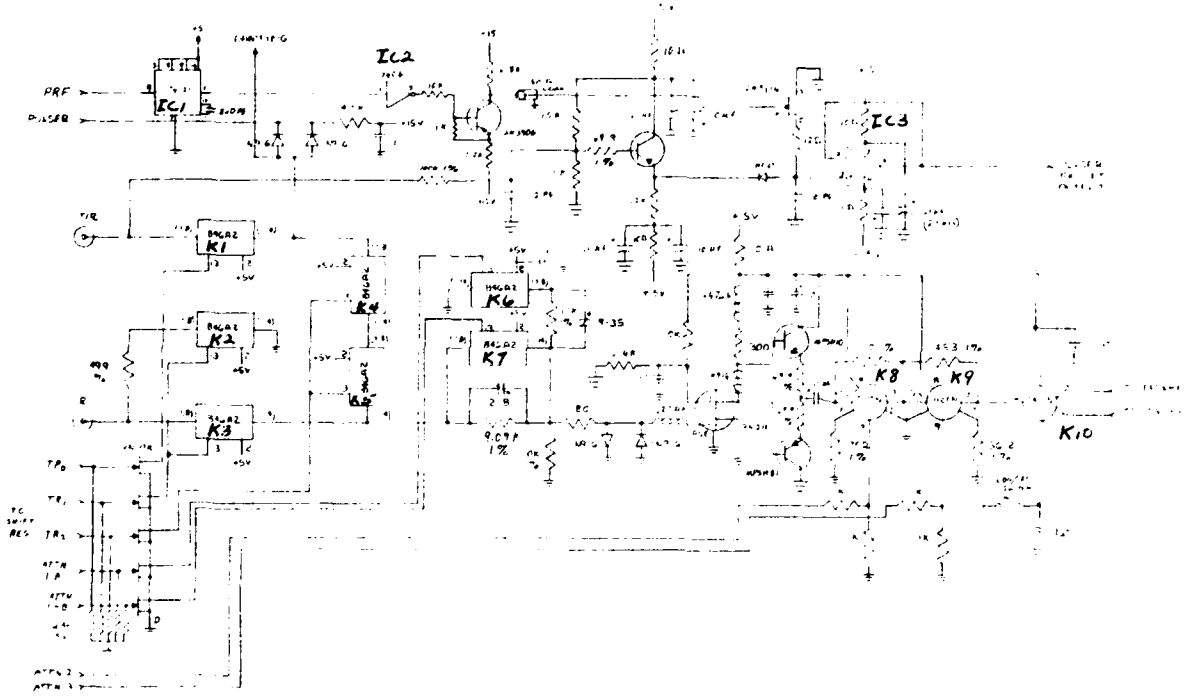



Figure 51. Amplifier Interface Schematic

mode. Relay K2 places a 50 ohm terminating resistor at the "R" input. In the "R" mode, relays K2 and K3 are selected. The pulser output is not connected to the T/R output in this mode. In the "OFF" mode, no relays will be selected and the T/R and R terminals will be isolated from the pulser/receiver.

The relays K6 and K7 select a high impedance attenuator, located before the preamplifier. The impedance of this attenuator is approximately 10K ohms. When selected, the input signal will be reduced by 20 dB. The relays K8 and K9 select the two attenuators after the preamplifier, 10 dB and 20 dB, respectively.

The preamplified RF signal is coupled to either the RF linear amplifier or the logarithmic amplifier through relay K10.

The control switch for K10 is located on the rear panel of the unit. The input to the logarithmic amplifier is selected when the switch provides a ground for pin 5 of K10.

## 19. FRONT PANEL INTERFACE, DISPLAYS, AND SWITCHES

The schematic for the front panel interface is shown in Figure 52. The interface provides for the routing of control and data signals between the microprocessor and the front panel. All front panel switches and displays are accessed as input/output (I/O) devices. The switches and displays are assigned specific addressing codes according to their group functions.

The control signals, $\overline{IO}$, $\overline{IOR}$, and $\overline{IOW}$ from the microprocessor, are decoded by a series of OR gates, IC 1 through IC 6. The decoded control signals are used to write data ($\overline{W}$) into the programmable panel displays and to read ($\overline{R}$) data from the panel switches. The $\overline{R}$ and $\overline{W}$ lines are also connected to the input of the open-collector buffers, IC 7 through IC 10. The output of the buffers are used to determine the direction of data flow between the microprocessor and the front

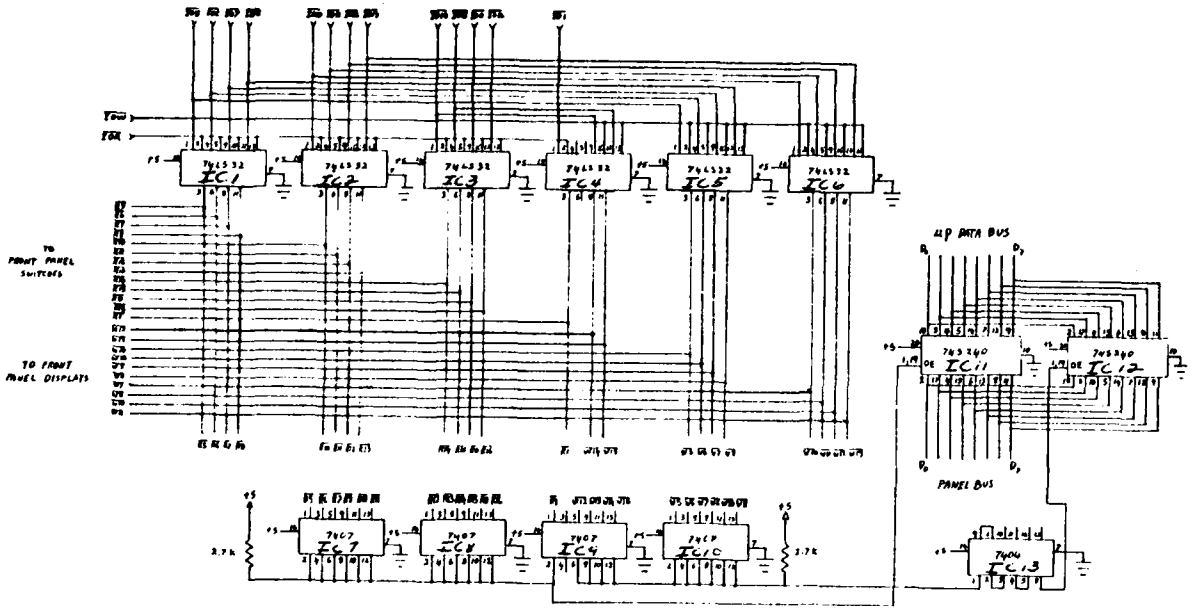



Figure 52. Front Panel Interface Schematic

panel. The octal three-state buffers, IC 11 and IC 12, provide the interface between the two bus systems. A small delay, IC 13, was added to insure adequate data setup times during the $\overline{W}$ cycle.

The schematic for the front panel displays is shown in Figure 53. The displays are hexadecimal type with on-board data latch and decoder. The data is latched into the displays during the rising edge of a $\overline{W}$ control pulse.

The schematic for the front panel switches is shown in Figure 54. The switches are mechanical rotary type with a common input line, 0, and four binary weighted outputs, 1, 2, 4, and 8. The $\overline{R}$ control lines are connected to the 0 inputs and will appear at the appropriate outputs according to the numerical value selected on the switch. The outputs of the switches are connected to the panel bus through the blocking diodes mounted on the back of the switches.

The schematic, shown in Figure 55, contains the circuitry for the pushbutton, mode control switches found on the front panel. When a switch is pushed, the $\overline{R}$ control signal is placed on the panel bus, through a blocking diode, and is then read by the microprocessor. The microprocessor determines which switch was selected by the data bit number assigned to each switch. The microprocessor will output the data bit that corresponds to the selected switch to the data hold latch IC 2. This will activate the display lamp associated with each switch. The display lamps for the reset and alter switches are not controlled by the microprocessor. The lamps are hardware activated by the dual timer IC 6.

## 20. SYNCHRONIZATION OUTPUT

The connector for the synchronization output is located on the rear of the back panel, BNC-type connector. The output is a synchronized internal system clock used as a timing reference for external devices and will drive a 50 ohm load at a pulse amplitude of

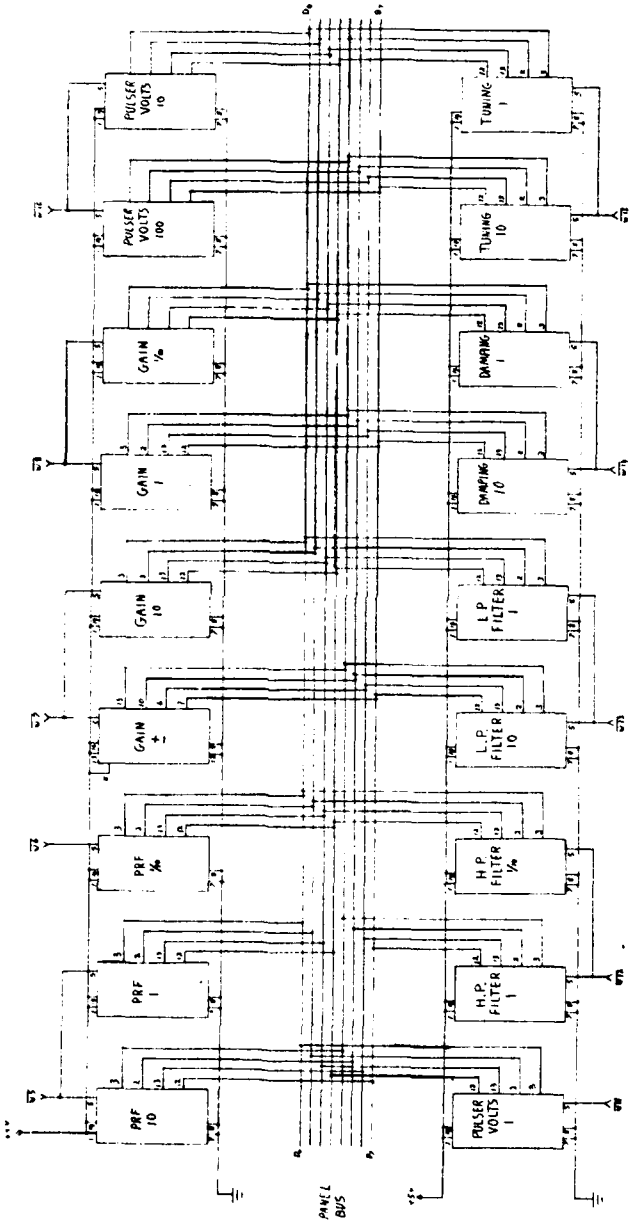



Figure 53. Front Panel Display Schematic

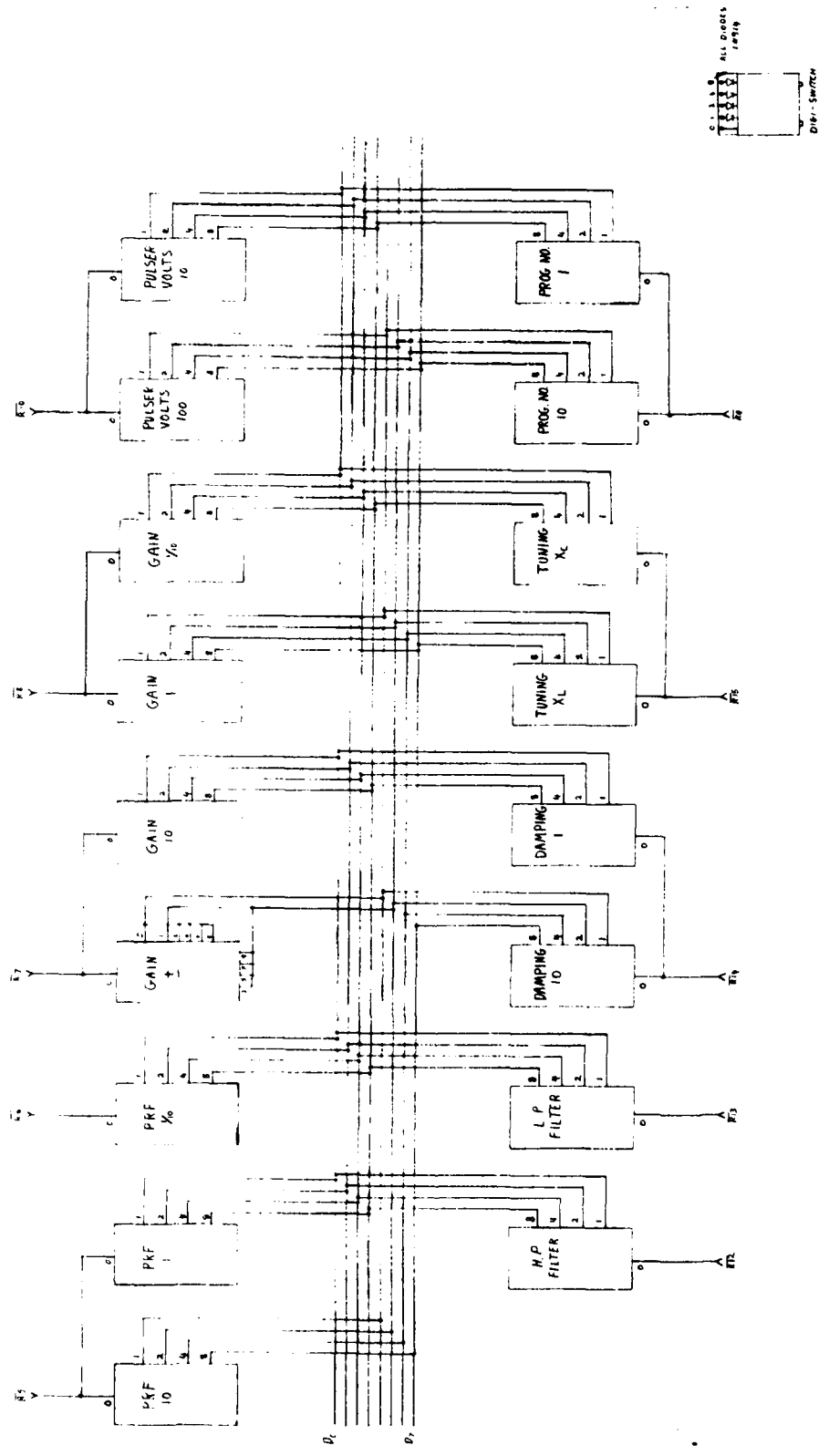



Figure 54. Front Panel Switch Schematic

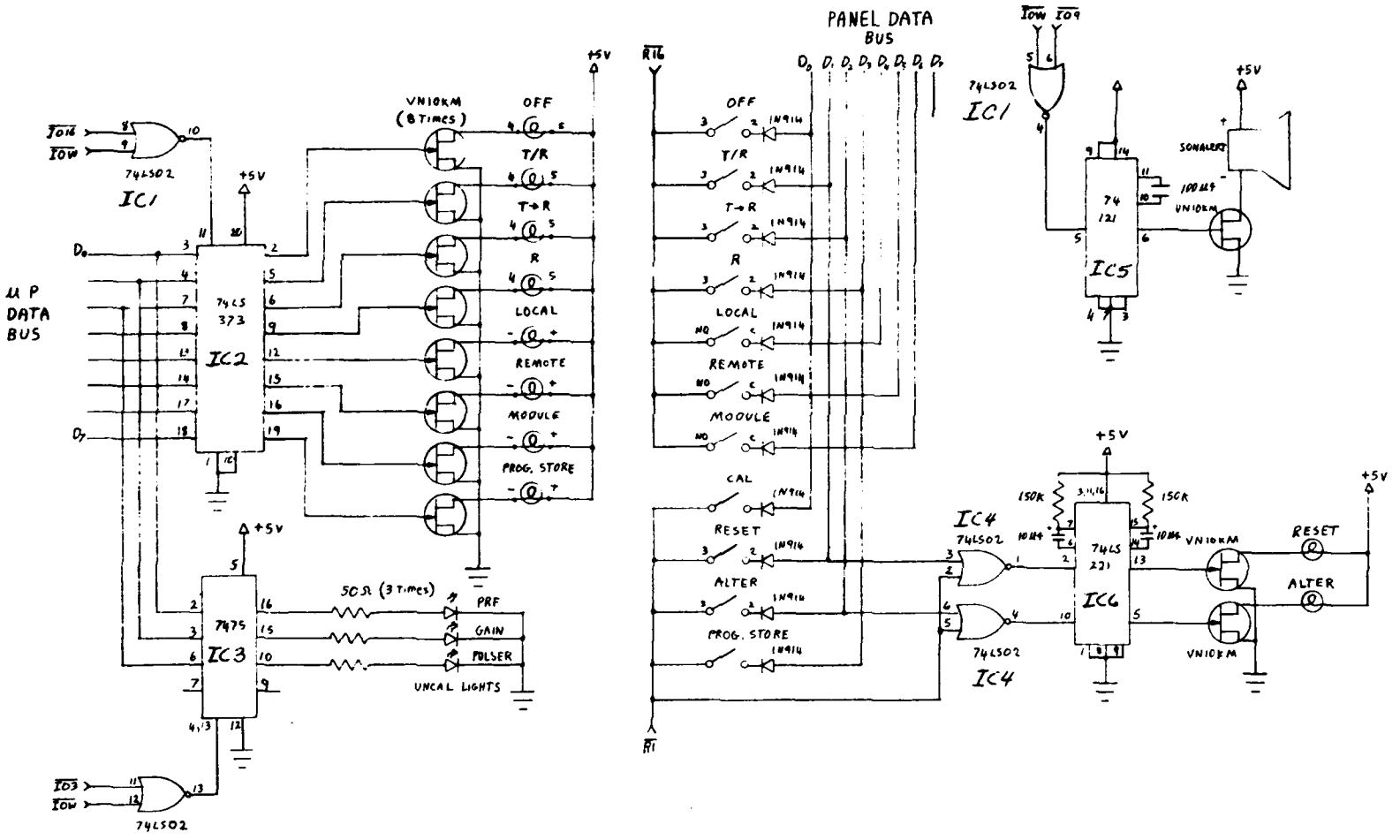
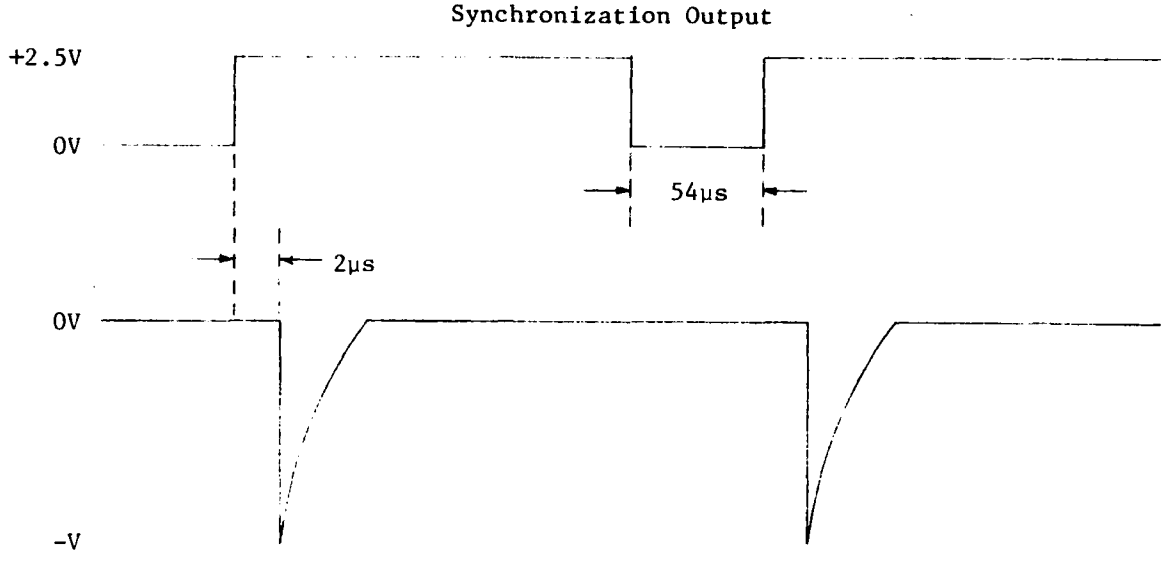



Figure 55. Front Panel Mode Control Schematic

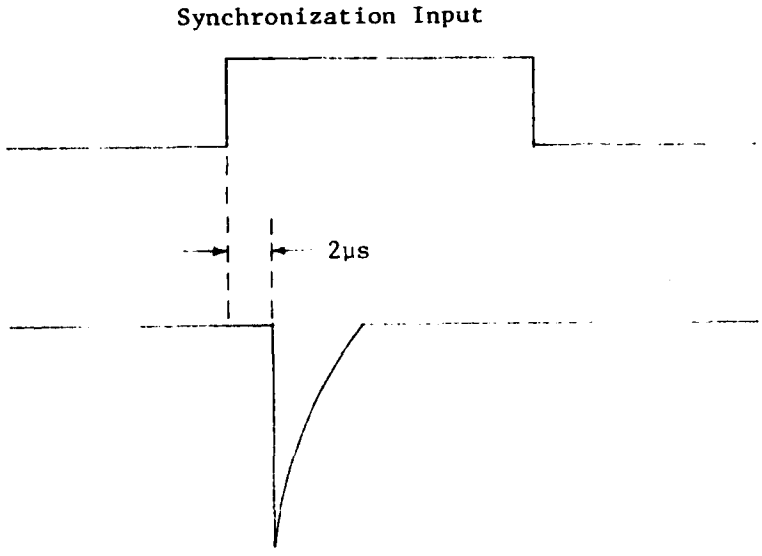
2.5 volts. The timing of the output pulse with respect to the transmitter pulse output is shown below.




Transmitter Pulse Output

21. SYNCHRONIZATION INPUT

The connector for the synchronization input is located on the rear of the back panel, BNC-type connector. The input is used when it is desired to operate the unit with an external clock generator. The input constitutes one TTL load and is only active when the front panel PRF switch is set to 000 Hz. The timing of the output transmitter pulse with respect to the input clock signal is shown on the following page.




## 22. REMOTE INTERFACE

A special internal and external instrumentation bus structure has been developed to be used in this instrument control application. The remote interface is compatible with the IEEE-488 computer interface standard. This interface allows for several functions:

- External control of front panel settings and displays.
- External control of instrument functions.
- Multiple instrument communication.
- Digital computer control of instruments.

Only digital information flow is allowed on this interface. It does not include other information, such as video signal, maintaining pulses, power supply lines, gate, etc. These are independent of the interface.

This interface has been designed to meet certain objectives. They include:

- Small number of lines (16) common to all devices connected to interface.

- Simple hardware implementation of interface, as few as three SSI or MSI chips required.

- Orderly transfer of bidirectional data flow.

- +5 volt logic family compatibility.

Definitions of the terms used to describe the bus structure are given below:

Interface - the term interface refers to the 16-line communication channel to which the instrument will be connected. This interface is used for digital information only.

Register - the term register is defined as a digital circuit capable of storing digital information. A register may be as small as a flip-flop or as large as a RAM. There are two general kinds of registers--those which have direct access to the interface and are called the interface registers and those within the instrument which are not connected to the interface in any way. These noninterface registers operate independently of the interface.

Local Mode - when a device is in the local mode, it has control of its own interface registers and is not in communication with any other instrument.

Remote Mode - when a device is in the remote mode, it loses control of its interface registers although it retains control of its own noninterface registers.

Controller - a controller is an instrument with the capability of reading from or writing into the interface registers of another instrument.

Active Controller - the device that is actually reading or writing data in another device is known as an active controller. Only one device may be the active controller at any time.

Master Controller - ultimate control of the interface resides with the master controller. It can regain control of the interface at any time even though another device may be the active controller. Only one device connected to the interface may be the master controller.

Device Address - each instrument connected to the interface has a unique 4-bit binary address. This address identifies the module with which the controller wishes to communicate.

Register Address - each interface register within an instrument has a unique 8-bit binary address. This address identifies the register in which the controller wishes to read or write.

Register Address Buffer - this buffer stores the 8-bit binary register address and is an interface register.

Service Request - when an instrument not in communication with the interface wishes to communicate with the controller, it issues a service request message.

Service Request Register - an interface register within an instrument that contains a code telling the controller the type of service which the instrument requires.

Service Action - the service action is the sequence of events which occurs after the controller has recognized the request of an instrument. The service action depends upon the content of the service request register.

Command Code Register - an interface register into which the controller writes a code commanding the instrument to take an action.

This interface is actually a communication channel between designated registers of each instrument. It allows one instrument to read or write in a register of another instrument, thus, allowing a transfer of data from one device to another. The nature of the data is not defined here, and it may be BCD data, instruction codes, etc.

The interface is not necessarily in contact with every register within an instrument. Only certain interface registers are designated to have access to the interface. For example, allowing the interface to have access to the display buffer registers and the switch matrix buffer will permit another device connected to the interface to have front panel switch and display control. Other registers within the device crucial to its operation may be left isolated from the interface.

It must also be stressed that the size of the register is left to the discretion of the designer. For example, only one flip-flop may be necessary to control a certain function. This interface is designed to allow the controller to write or set any number of bits.

The interface allows two devices to be in communication at one time. In all communication situations, one device is the controller, and the other is the slave (remote mode); any other units on the bus can remain in the local mode. The controller handles the direction of data flow, determining which registers within the remote module will be accessed.

Control of the interface may be passed from one device to another. However, it must be remembered that the definition of control does not state that a device controlling the interface has the power to independently control the course of events on the interface. Rather, it only implies that a controlling device may efficiently direct the flow of data for a definite preprogrammed period of time. The ultimate control of the interface lies with the master controller which may at any time invoke immediate control of the interface.

It must be emphasized that the interface and associated devices are in a dynamic condition. The control of the interface passes from one device to another as the need to communicate changes. However, ultimate control always remains with the master controller.

A detailed description of the control-bus structure follows.

Interface Lines

| | | |
|---|---|---|
| | Bus 7 | |
| | 6 | |
| | 5 | |
| (3 state) | 4 | 8 Lines of Data Address Bus |
| | 3 | |
| | 2 | |
| | 1 | |
| | Bus 0 | |
| | $\overline{\text{DAV}}$ | Data Valid |
| | $\overline{\text{NRFD}}$ | Not Ready for Data |
| | $\overline{\text{NADC}}$ | Not Data Accepted |

| | |
|---|---|
| $\overline{SRQ}$ | Service Request |
| $\overline{EOI}$ | End of Identify |
| $\overline{IFC}$ | Interface Clear |
| $\overline{ATN}$ | Attention |
| $\overline{REN}$ | Remote Enable |

Bus 7 - Bus 0 - Data Address Bus - the 8 bits of the data address bus are used for the flow of all data and addresses within the interface. It is bidirectional, allowing information to flow in either direction between two communicating devices.

Bus is necessary for all devices which will be connected to the interface.

Control Bus - the control bus consists of eight lines and is used to signal which devices are to be in communication on the bus. It controls the flow of data in an orderly manner. The bus also allows for the transfer of interface control from one device to another. The lines making up the control bus are bidirectional. However, not all devices necessarily will use these lines in both directions. Some devices will not require certain of these lines for proper communication with the interface. Each of these control lines will be described.

$\overline{DAV}$--Data Valid - is a GPIB handshake control line. It indicates the availability and validity of information on the Data-Address Bus.

$\overline{\text{NRFD}}$--Not Ready for Data - is a GPIB handshake control line. It indicates the condition of readiness of the device(s) connected to the bus to accept data.

$\overline{\text{NADC}}$--Not Data Accepted - is a GPIB handshake control line. It indicates the condition of acceptance of data by the device(s) connected to the bus.

$\overline{\text{SRQ}}$--Service Request - is a GPIB command line. It indicates the need for attention and requests an interruption of the current sequence of events on the GPIB.

$\overline{\text{EOI}}$--End of Identify - is a GPIB command line. It indicates the end of a multiple byte transfer sequence or, in conjunction with the ATN line, addresses the device during a polling sequence.

$\overline{\text{IFC}}$--Interface Clear - is a GPIB command line. It places the interface functions in a known quiescent state.

$\overline{\text{ATN}}$--Attention - is a GPIB command line. It specifies how data on the Data Address Bus lines are to be interpreted.

$\overline{\text{REN}}$--Remote Enable - is a GPIB command line. It selects (in conjunction with other messages) remote or local control of the device.

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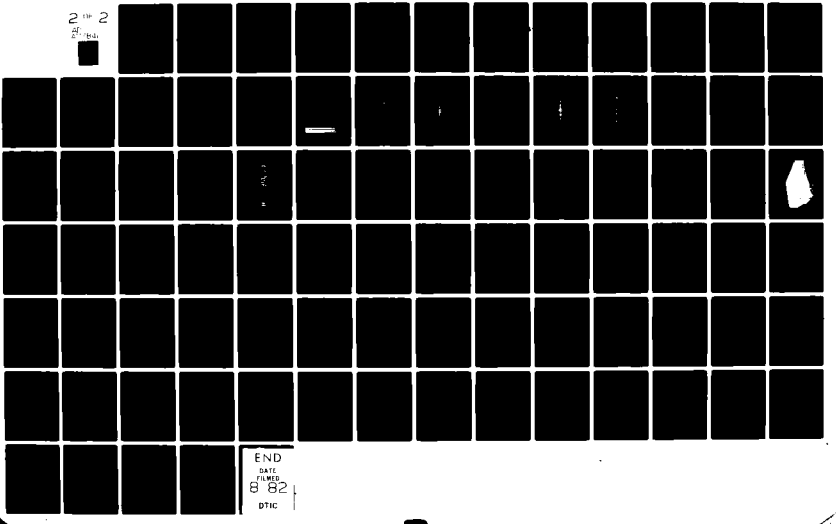
ADVANCED NONDESTRUCTIVE EVALUATION (ULTRASONIC PULSER/RECEIVER --ETC(U)
MAY 82 R A SHAUFL F33615-79-C-5020
UNCLASSIFIED AFWAL-TR-81-4038 NL



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The connector for the remote interface is located on the rear panel of the instrument. It is a 50-pin, D-type connector and the designation of the pins are as follows:

| | | | | | |
|---|---|---|---|---|---|
| Pin | 1 | Gnd | Pin | 26 | $\overline{\text{EIO}}$ |
| | 2 | Gnd | | 27 | Gnd |
| | 3 | $\overline{\text{NADC}}$ | | 28 | $\overline{\text{REN}}$ |
| | 4 | Gnd | | 29 | n/c |
| | 5 | $\text{DIO}_6$ | | 30 | n/c |
| | 6 | Gnd | | 31 | n/c |
| | 7 | $\text{DIO}_3$ | | 32 | n/c |
| | 8 | $\text{DIO}_1$ | | 33 | n/c |
| | 9 | Gnd | | 34 | Gnd |
| | 10 | $\overline{\text{IFC}}$ | | 35 | $\overline{\text{NRFD}}$ |
| | 11 | Gnd | | 36 | Gnd |
| | 12 | n/c | | 37 | $\text{DIO}_7$ |
| | 13 | n/c | | 38 | Gnd |
| | 14 | n/c | | 39 | $\text{DIO}_4$ |
| | 15 | n/c | | 40 | Gnd |
| | 16 | n/c | | 41 | Gnd |
| | 17 | n/c | | 42 | $\text{DIO}_0$ |
| | 18 | $\overline{\text{DAV}}$ | | 43 | Gnd |
| | 19 | Gnd | | 44 | $\overline{\text{ATN}}$ |
| | 20 | $\overline{\text{SRQ}}$ | | 45 | Gnd |
| | 21 | Gnd | | 46 | n/c |
| | 22 | $\text{DIO}_5$ | | 47 | n/c |
| | 23 | Gnd | | 48 | n/c |
| | 24 | $\text{DIO}_2$ | | 49 | n/c |
| | 25 | Gnd | | 50 | n/c |

## 23. SELF-CALIBRATION

The requirement for self-calibration within the pulser/receiver system was addressed in two functional areas; pulser repitition rate (PRF) and pulser output amplitude. The microprocessor is incorporated as the main determining element within a closed loop control.

The PRF was selected for self-calibration to insure repeatable, accurate, no drift system timing pulses. These parameters are essential for the digital sampling and signal averaging of the received analog waveforms. The stability and accuracy of the PRF is determined by the crystal controlled oscillator found in the PRF counter circuit. The crystal was selected to maintain a 10 Hz tolerance over a wide temperature range. The output of the PRF counter is read by the microprocessor and compared to the selected PRF. If the comparison is within the 10 Hz tolerance, the microprocessor will display the PRF that was selected. If the comparison shows an out-of-tolerance condition, the microprocessor will implement a calibration routine until the output of the PRF counter reads within the tolerance specified.

The software calibration routine initiates an incremental or decremental code change to the PRF generator until the PRF is within tolerance. In the advent that the selected PRF cannot be reached, the microprocessor will indicate an out-of-calibration condition, via the uncal light on the front panel.

The output from the PRF counter may also be utilized as the calibration feedback for an external PRF input. The PRF counter will automatically read an external PRF input when the PRF switch, on the front panel, is placed to the 000 Hz position. The front panel display will indicate the measured external PRF input. This information is also available through the remote interface bus (GPIB-488).

The output amplitude of the pulser was selected for self-calibration to eliminate the problem of transducer excitation uncertainty. Typically, the output amplitude from a standard exponential type pulser will vary as much as 6 dB when subjected to load and tuning variations. A high voltage pulser, such as the one designed for this program, could possibly damage a transducer if the excitation pulse amplitude were not known and controlled.

The pulser supply and pulser output measurement and control circuits were developed for the control and monitor elements in the self-calibration loop. The microprocessor was intended to be utilized to close the loop by providing the appropriate processed correction feedback.

The pulser output is scaled down, peak detected, and converted into digital information by the pulser measurement circuit. This digital representation of the pulse amplitude is processed by the microprocessor and displayed on the front as the pulser volts. The information was also intended to be used as feedback to correct for any differences between the pulser volts switch setting and the measured pulse amplitude. The software algorithm, developed to close the self-calibration loop, produced to a low frequency oscillation (hunting) effect on the pulser output amplitude. This condition was not sufficiently corrected, and the self-calibration feedback loop was not closed.

## 24. EVALUATION

The pulser/receiver has been evaluated to show: (1) the flaw detection capabilities and (2) the signal resolution capabilities of the unit.

The pulser/receiver was evaluated for flaw detection capabilities on a #7075-1-300 standard test block. The ultrasonic linear return from the #1 Flat Bottom Hole was recorded as shown in Figure 56. The output voltage level is approximately 4 volts peak-to-peak, and the noise level is greater than -28 dB from the amplified return. A similar recording was made of the logarithmic output as shown in Figure 57.

The pulser/receiver was evaluated for near surface resolution. A flat stainless steel test plate was used for the evaluation. The results and test parameters for the linear receiver output and the

logarithmic receiver output were recorded as shown in Figures 58 through 61. The results clearly show the fast recovery and low distortion of the ultrasonic amplifiers.

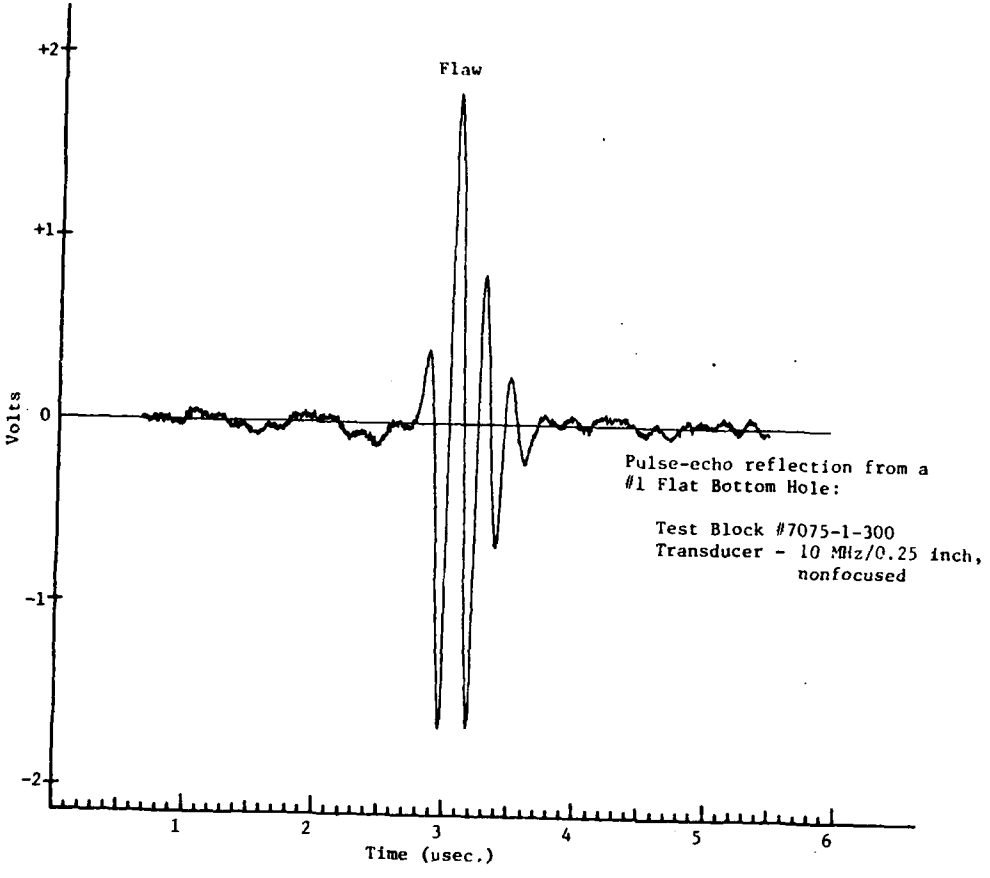


Figure 56. Pulser/Receiver Linear Evaluation Plot

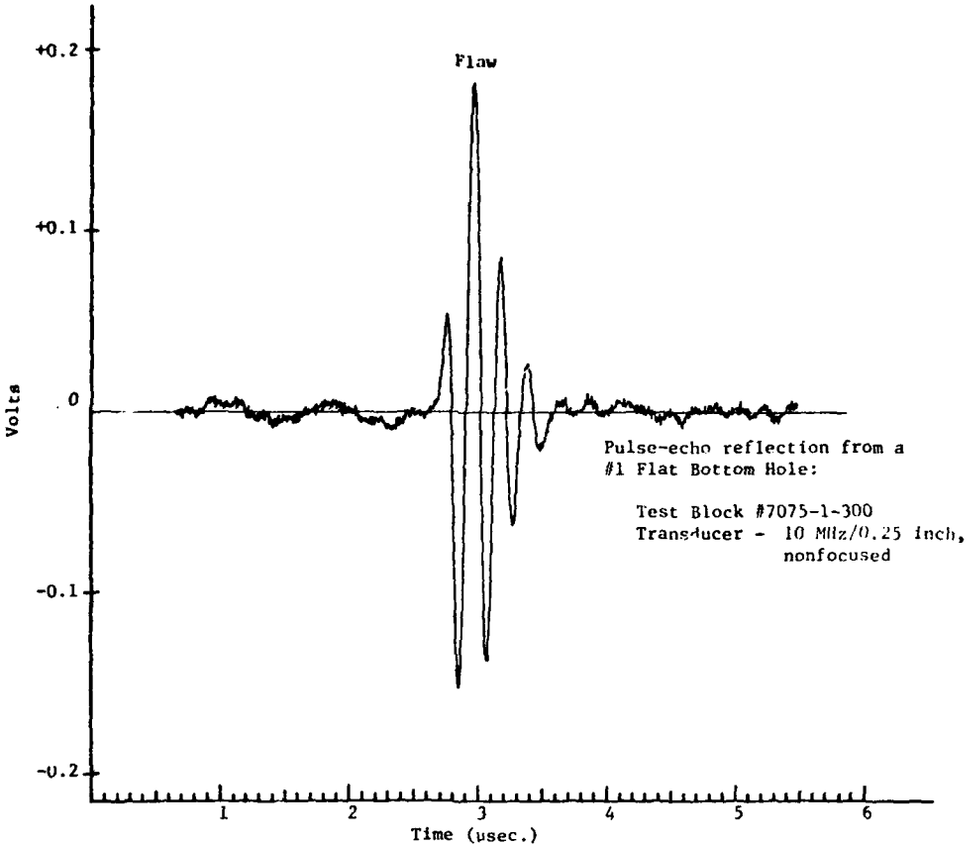


Figure 57. Pulser/Receiver Logarithmic Evaluation Plot

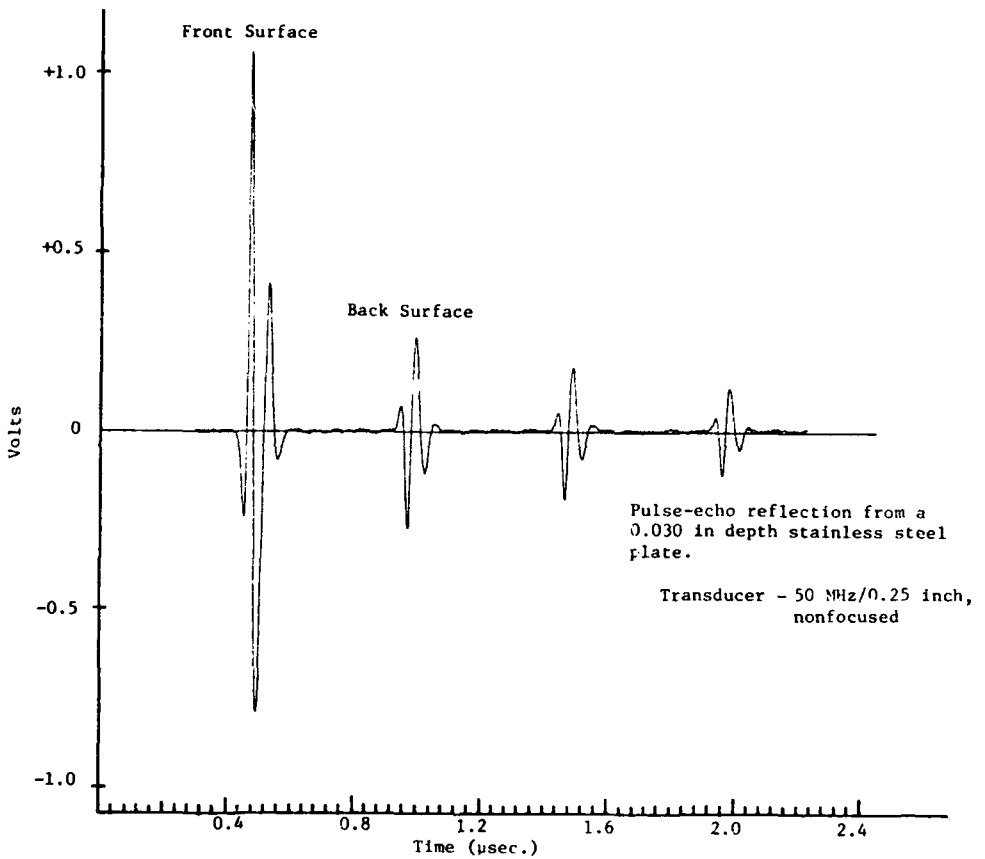


Figure 58. Pulser/Receiver Linear Evaluation Plot

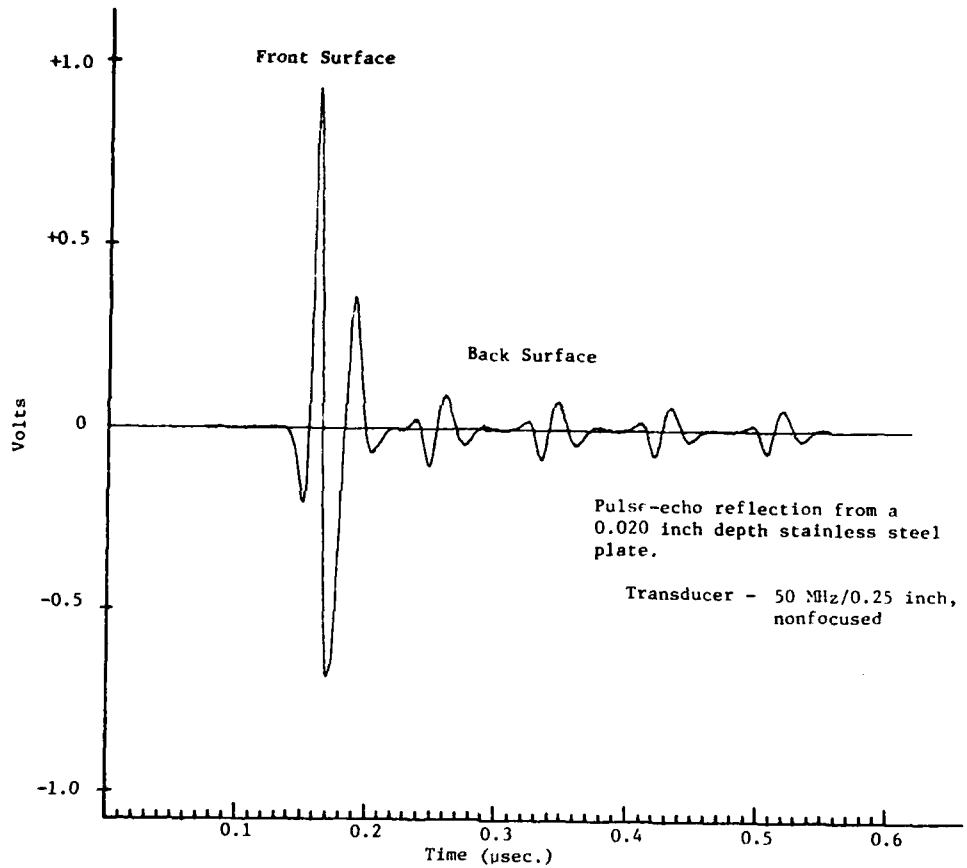


Figure 59. Pulser/Receiver Linear Evaluation Plot

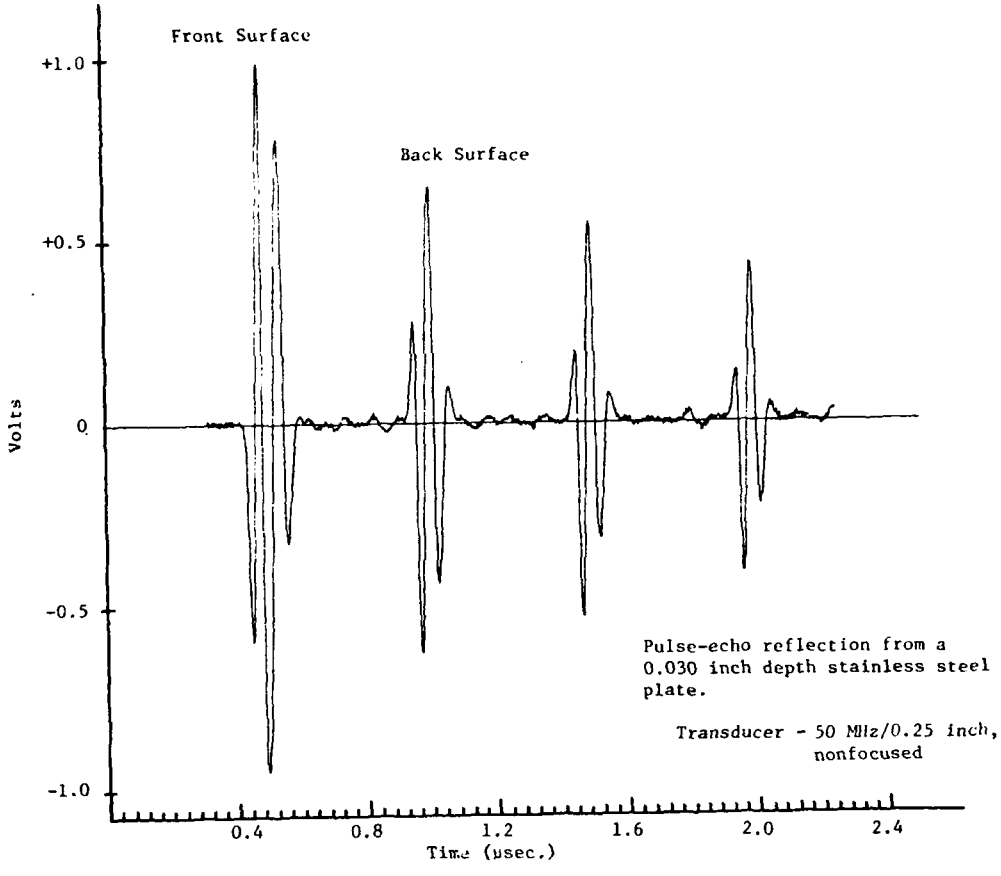


Figure 60. Pulser/Receiver Logarithmic Evaluation Plot

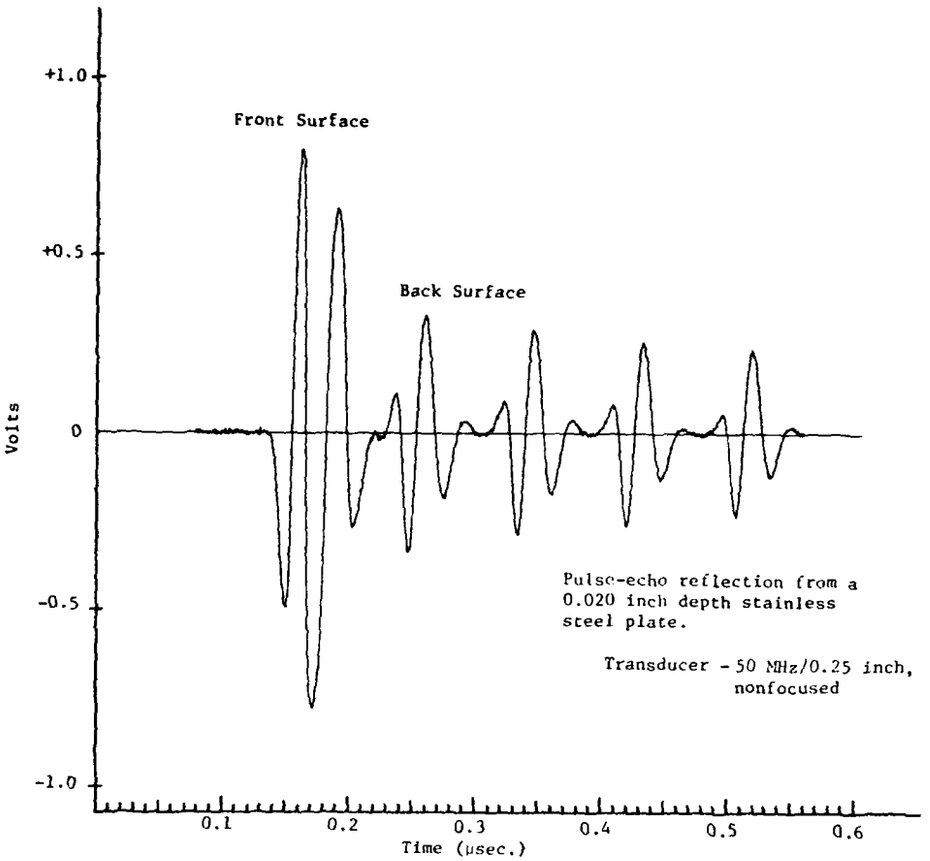


Figure 61. Pulser/Receiver Logarithmic Evaluation Plot

## SECTION IV

## PSEUDORANDOM-BINARY-SIGNAL CORRELATION SYSTEM

### 1. PRIMARY FUNCTION

Correlation techniques are widely used in communications, instrumentation, computers, telemetry, sonar, radar, medical, and other signal processing systems. Correlation has several desirable properties including:

- The ability to detect a desired signal in the presenc f noise or other signals.
- The ability to recognize specific patterns within an or digital signals.
- The ability to measure time delays through various media.

As these properties indicate, correlation is essentially a comparison process. The correlation between two functions is a measure of their similarity. This comparison can be expressed mathematically as the correlation between two functions $v_1(t)$ and $v_2(t)$:

$$R_{12}(T) = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} v_1(t)\, v_2(t + T)\, dt \qquad (5)$$

Here, $R_{12}(T)$ refers to the correlation between two signals, $v_1$ and $v_2$. It is determined by multiplying one signal, $v_1(t)$, by the other signal shifted in time, $v_2(t + T)$, and then taking the integral of the product. Thus, correlation involves multiplication, time shifting (or delay), and integration.

If the functions are periodic, the expression simplifies to:

$$R_{1,2}(\tau) = \frac{1}{T_0} \int_{-T_0/2}^{+T_0/2} v_1(t)\, v_2(t + \tau)\, dt \qquad (6)$$

where $T_0$ is the period of the functions.

The effects of multiplication, time shifting, and integration can be visualized graphically in Figure 62. This particular example shows two waveforms that have similar shapes and equal periodicity. The figure shows one particular time shift, $\tau_0$, between $v_1(t)$ and $v_2(t + \tau)$. In this example, $\tau_0$ was chosen to yield a very low correlation between the two functions.

A value of $\tau_0$ selected to maximize the degree of overlap between the two functions would yield maximal correlation. As this example illustrates, the correlation of two functions is very sensitive to their relative phasing.

The correlation of a function with a time-delayed replica of itself is called autocorrelation. Thus, $v_1(t) = v_2(t)$ and $R_{1,2}(\tau)$ becomes $R(\tau)$ and is given by:

$$R(\tau) = \frac{1}{T_0} \int_{-T_0/2}^{+T_0/2} v_1(t)\, v_1(t + \tau)\, dt \qquad (7)$$

## 2. COMPUTER MODEL

A computer model was developed which would evaluate the feasibility of performing a 1-bit cross correlation on each output bit of an 8-bit analog-to-digital converter (ADC). The output from each correlator would then be summed after weighting with the appropriate binary bit weight. It was believed this approach would result in an increased linearity at signal-to-noise ratio $S/N > 1$.

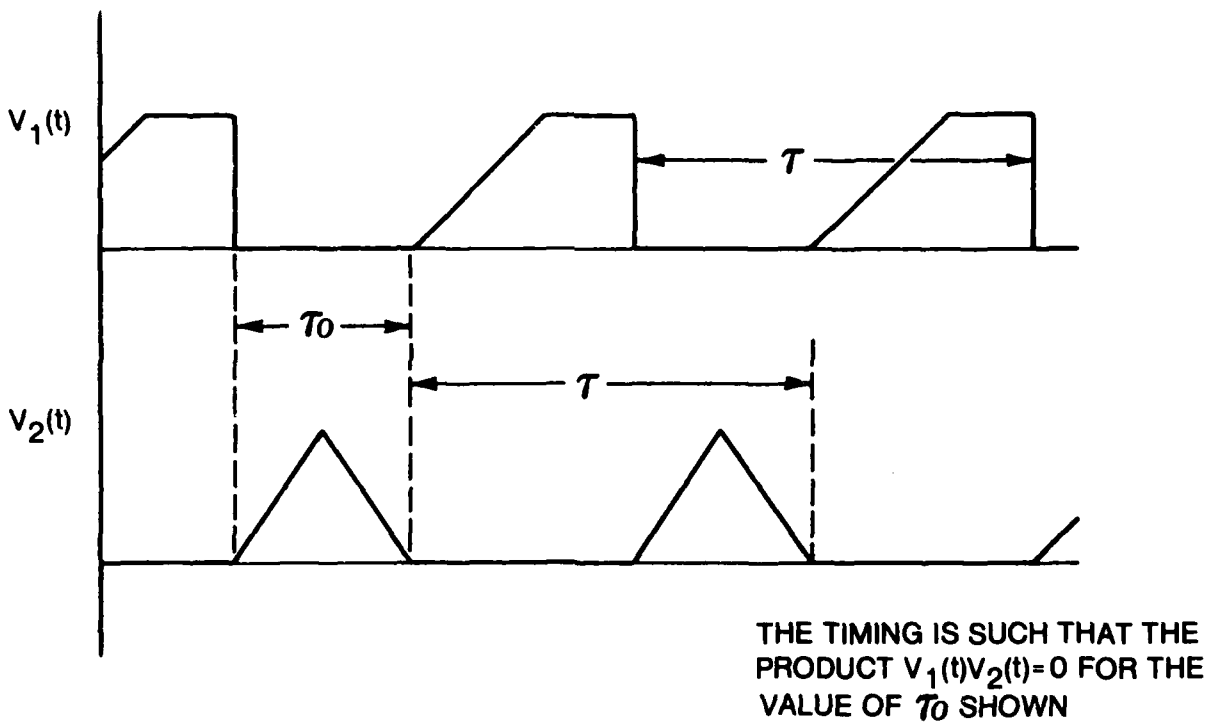


Figure 62. Correlation of Two Functions

The model was also designed to perform signal averaging of the correlator output from independe[illegible] realizations of the pseudorandom sequence. The parameters burst length, delay, amplitude, transducer frequency, sample frequency, number of ADC bits, and additive Gaussian noise variance were all variables capable of being changed through menu prompting.

When analyzing time varying signals which have some type of associated random variation, the term stochastic process[1] is used to describe such signals. A stochastic process describes an ensemble of all possible realizations of the process. A zero mean stochastic process will have a given realization with the maximum likelihood value of the mean being zero, although the mean of one realization may not, in fact, be zero. If the stochastic process is discrete, the term sequence is often used rather than process[2]. Further, if the random behavior has a long range periodicity, the sequence will be referred to as a pseudorandom stochastic sequence or simply a pseudorandom sequence.

The model first computed an idealized transducer impulse response h(nT) using the expression

$$h(nT) = e^{-\left(\frac{nT - \delta}{w}\right)} \cos w(nT - \delta)$$

where $T = 1/f_s$ is the reciprocal sampling rate, $\delta$ is the delay, and w is the pulse duration term, all in units of msec. This idealized impulse response was intended to represent a sampled (not quantized)

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[1]Breipohl, A. M., Probabilistic Systems Analysis (John Wiley and Sons, Inc., New York, 1970), pp. 273-333.

[2]Meditch, J. S., Stochastic Optimal Linear Estimation and Control (McGraw-Hill Book Co., New York, 1969), pp. 118.

analog signal and was, therefore, computed and stored in a floating-point array. A discrete Fourier transform of the impulse response could then be requested which would verify whether any significant aliasing had occurred, allowing modification of the impulse response parameters.

A realization of the pseudorandom sequence could be computed in a similar manner using the expression

```
x(nT) = FLOAT(2*IFIX(RAN(ID1,ID2)+0.5)-1)
```

This expression generated a zero mean pseudorandom sequence with a uniformly distributed probability density function of amplitude 1/2 extending from -1 to +1.

The pseudrandom sequence and the transducer impulse response were computed in order to obtain the response y(nT) to a particular realization of the pseudorandom sequence. This response was obtained by the convolution h(nT) * x(nT). The discrete convolution can be expressed as

$$y(n) = \sum_{k=-\infty}^{\infty} h(k)\, x(n-k)$$

If the sequences are assumed to be causal [i.e., $h(k) = x(k) = 0$ for $k < 0$], the convolution sum can be evaluated using a discrete Fourier transform (DFT). The DFT can then be implemented using a highly time efficient algorithm called a fast Fourier transform (FFT). In this way, the transducer response can be computed for each individual realization of the pseudorandom sequence.

The y(nT) response is representative of the analog pulse-echo ultrasonic signals which are correlated with the pseudorandom sequence. The pseudorandom sequence is 1-bit digitized and stored in a fixed point array to be used as the reference code to be correlated

with the M-bit digitized y(nT) sequence which is stored in an M x N fixed point array. The term M is the number of bits in the digitization, and N specifies the total number of points (1024 maximum). The digitization is equivalent to an ADC and is achieved using successive approximation and integer operations, testing and storing each bit value in the M x N array. Each column of the M x N array corresponds to a new pseudorandom sequence which is correlated with the reference signal using an exclusive $\overline{OR}$ for a multiplier. Each of the M, 1 x N columns are weighted with $2^m$ ($0 \leq m \leq M$) and summed to form the final correlated output.

The operations described thus far can all be performed repetitively with statistically independent realizations of the pseudorandom sequence. The correlated outputs from each pass can be summed resulting in a signal averaged output. This provision is included to allow testing of the effect of signal averaging on the signal-to-sidelobe ratio and linearity.

Figure 63 shows an idealized transducer response. This response is convolved with the pseudorandom sequence realization shown in Figure 64. The convolved output is shown in Figure 65. This output is then digitized with a 1-bit ADC and correlated with digitized pseudorandom sequence realization to obtain the correlated output shown in Figure 66. This same process was also attempted for M-bit digitization where $1 \leq M \leq 7$. This correlation procedure failed on all but the 1-bit digitization. The model indicated an output in the time region of the ultrasonic burst but the sense of the transducer impulse response was totally lost.

It is believed this failure was the result of the inherent nonlinearity of the binary coding operation which could not be restored by the linear superposition operation of simply weighting and summing the outputs from each bit. Based on these results the decision was made to discontinue the initial approach and concentrate on the 1-bit digital design.

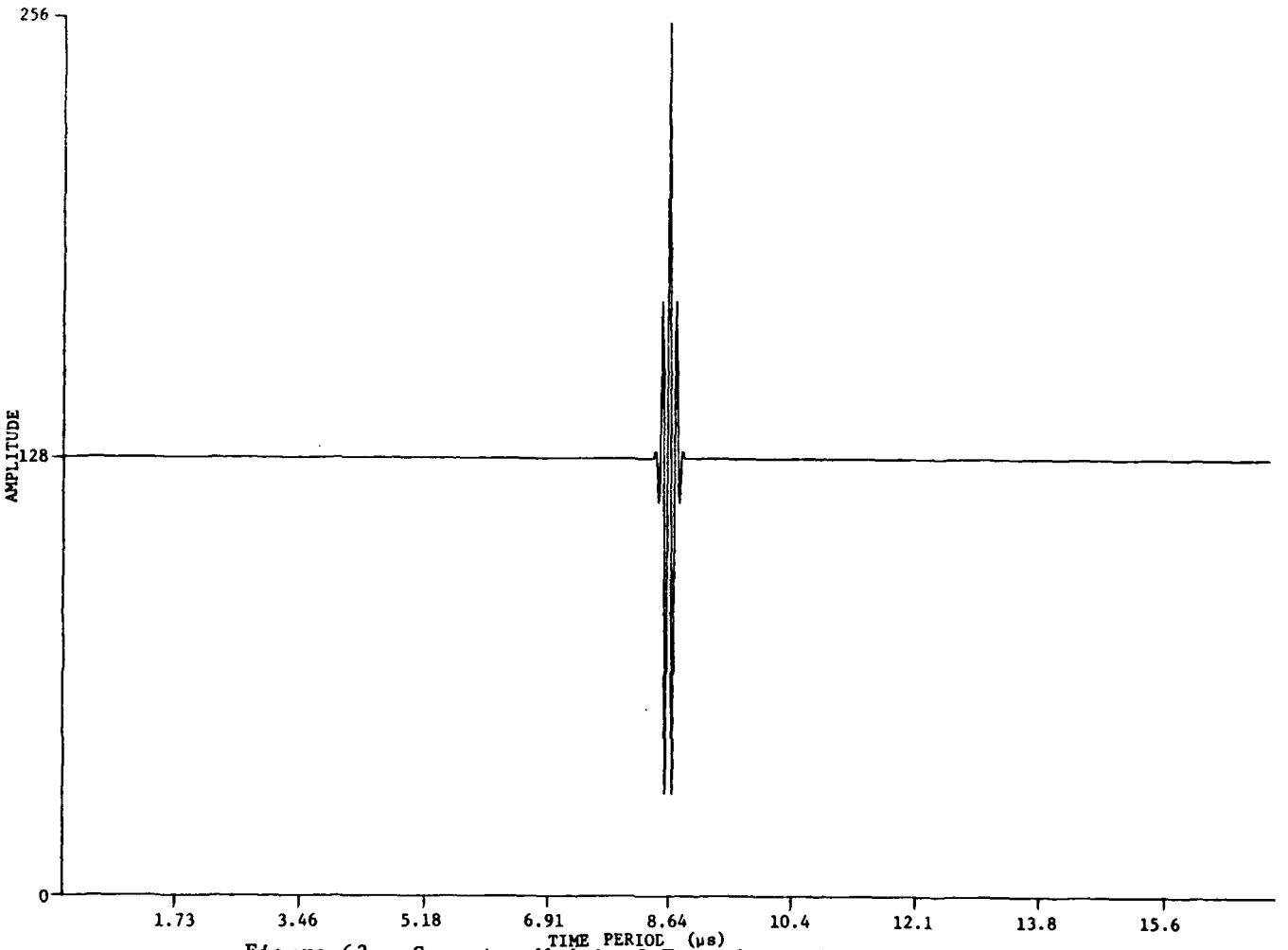


Figure 63. Computer Model of Transducer Impulse Response

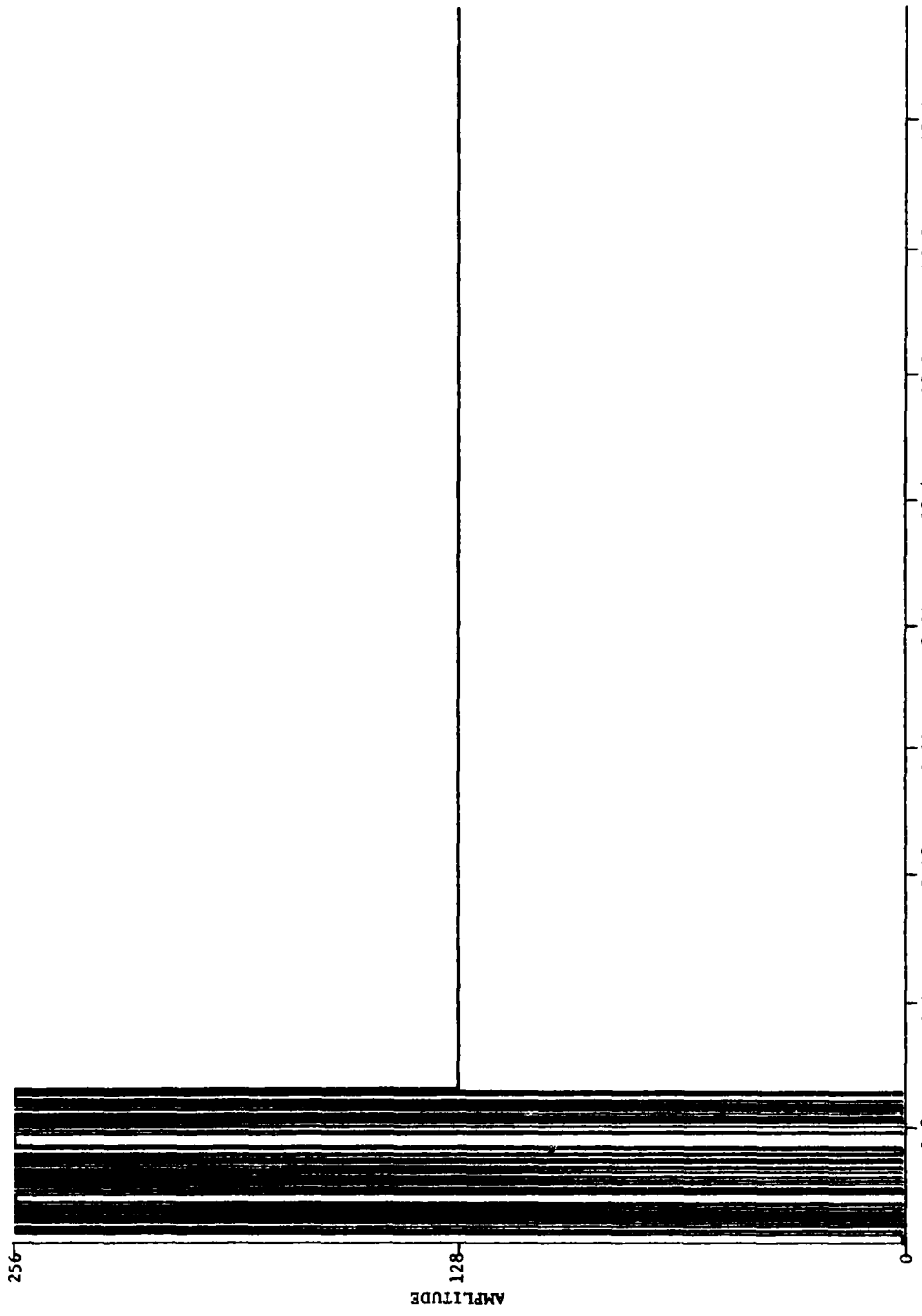


Figure 64. Computer Model of Pseudorandom-Binary Sequence

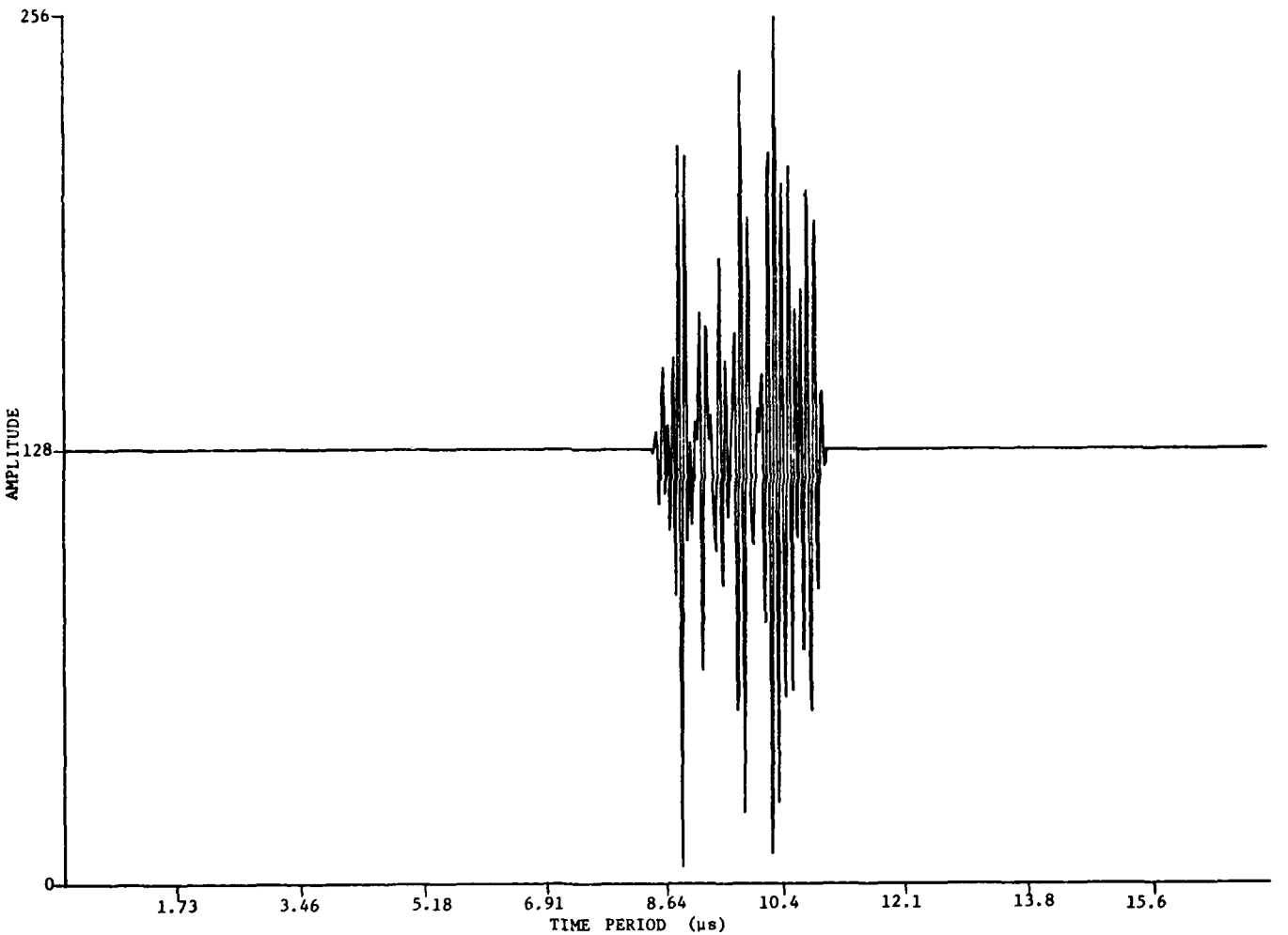


Figure 65. Computer Model of Convolution

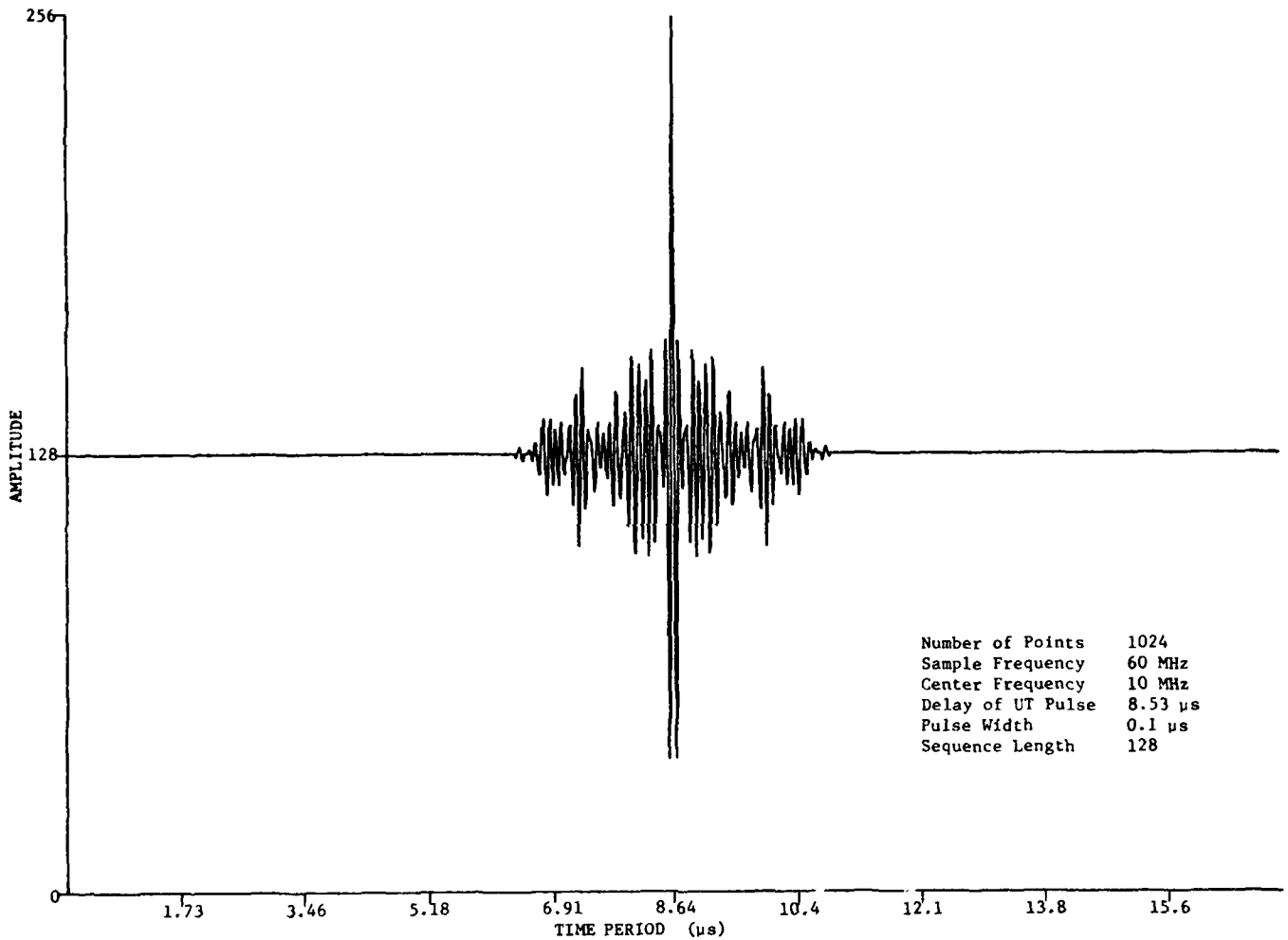


Figure 66. Computer Model of Correlation

Figures 67 and 68 show outputs from a 1-bit correlator model for increasing sequence lengths. As can be seen from these figures, the signal-to-sidelobe ratio increases as the pseudorandom sequence length increases. The output linearity and reduction in signal-to-sidelobe ratio as a function of the number of signal averages was investigated using the known impulse response shown in Figure 69. This impulse response consisted of a superposition of seven pulses with the initial pulse delayed 2.0 μsec and each subsequent pulse delayed 1.0 μsec from the preceding one. The relative peak pulse amplitudes were 1.0, 0.8, 0.6, 0.4, 0.2, 0.01, and 0.001. Figure 70 is typical of the response y(nT) resulting from the convolution of the impulse response and a particular realization of the pseudorandom sequence of length ~ 4.27 μsec (256 points).

Figures 71 to 74 are the signal averaged correlated outputs from the model with the number of averages varied through 2, 4, 16, and 256 averages. These results indicate that the signal-to-sidelobe ratio is increasing as the number of averages is increased. It is believed this improvement is proportional to the square root of the number of averages although no quantitative measure was performed. These same figures also indicated that signal averaging has little effect on the linearity of the corelation (i.e., it is equally nonlinear independent of signal averaging).

The correlated output of Figure 74 clearly indicates the nonlinearity of the 1-bit correlator. The last two pulses deviate from a linear response by 30.2 dB and 49.4 dB, respectively, with the deviation increasing as the signal becomes smaller. This output was obtained with no additive Gaussian noise on the input, although a noise floor of approximately -150 dB is assumed because a single precision floating point number is expressed with a 24-bit fractional part in a DEC LSI-11 which introduces this quantization error[1].

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[1]Oppenheimer, A. V. and Schafer, R. W., Digital Signal Processing (Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1975), pp. 417.

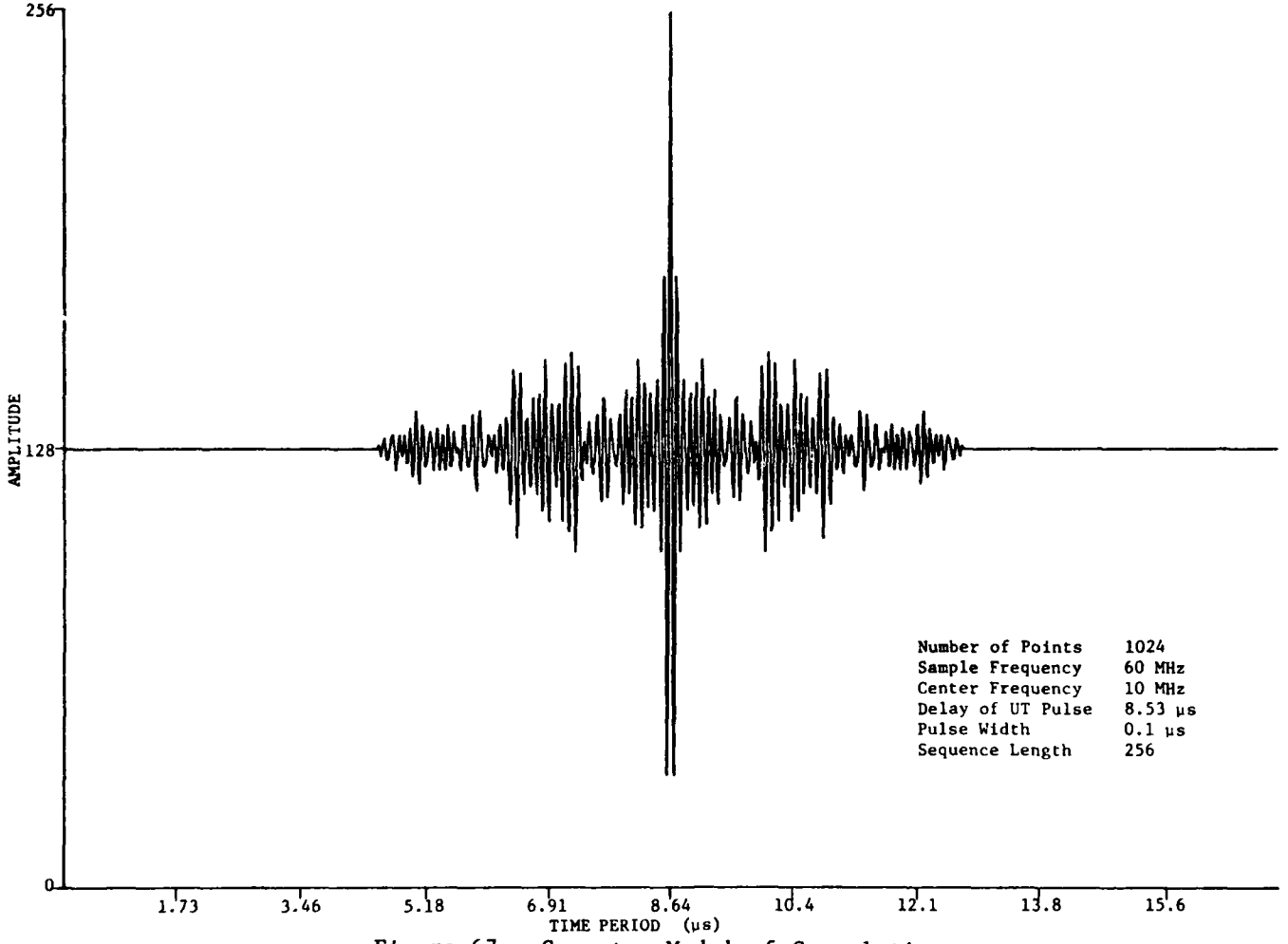


Figure 67. Computer Model of Correlation

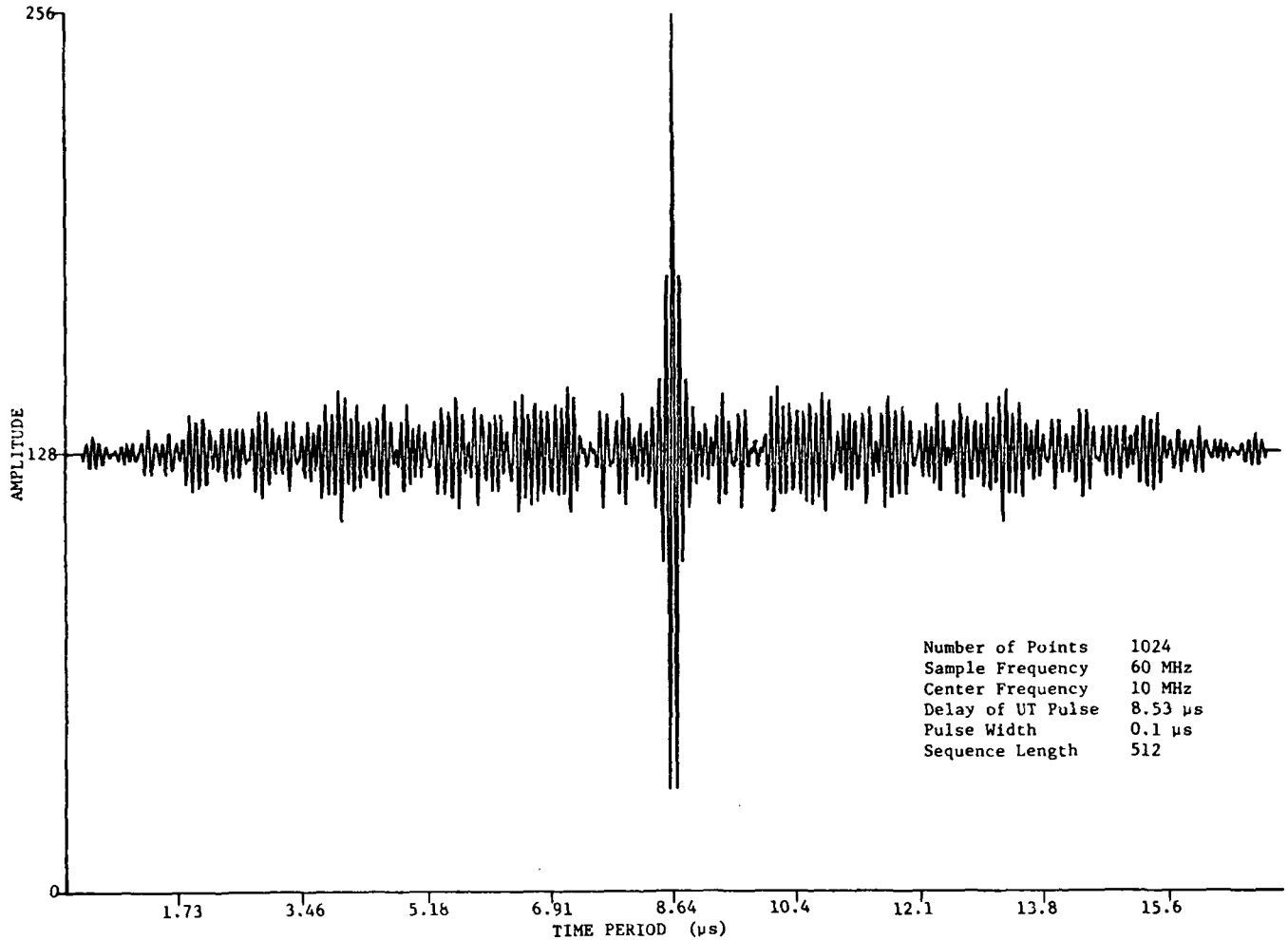


Figure 68. Computer Model of Correlation

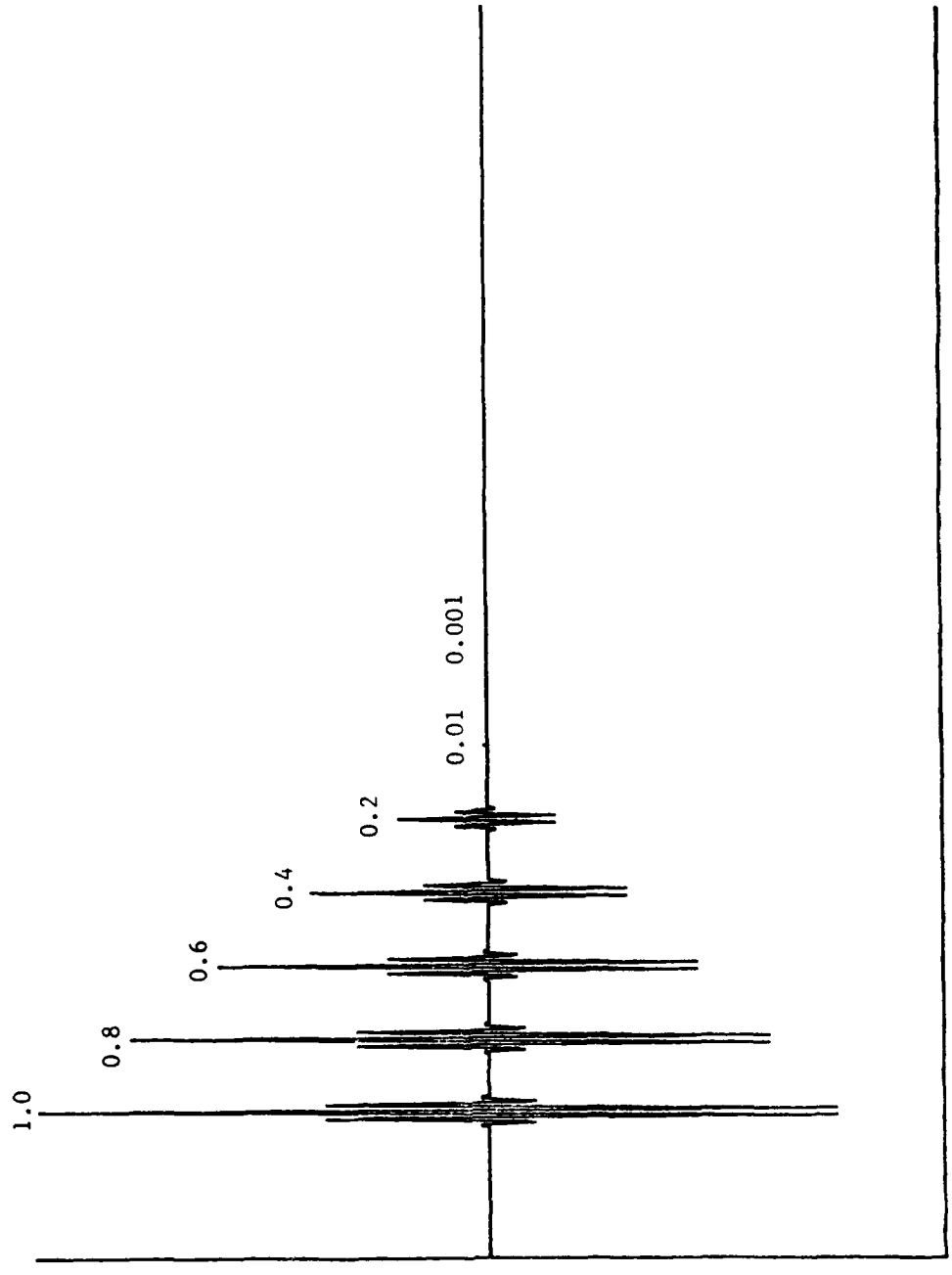


Figure 69. Known Impulse Response

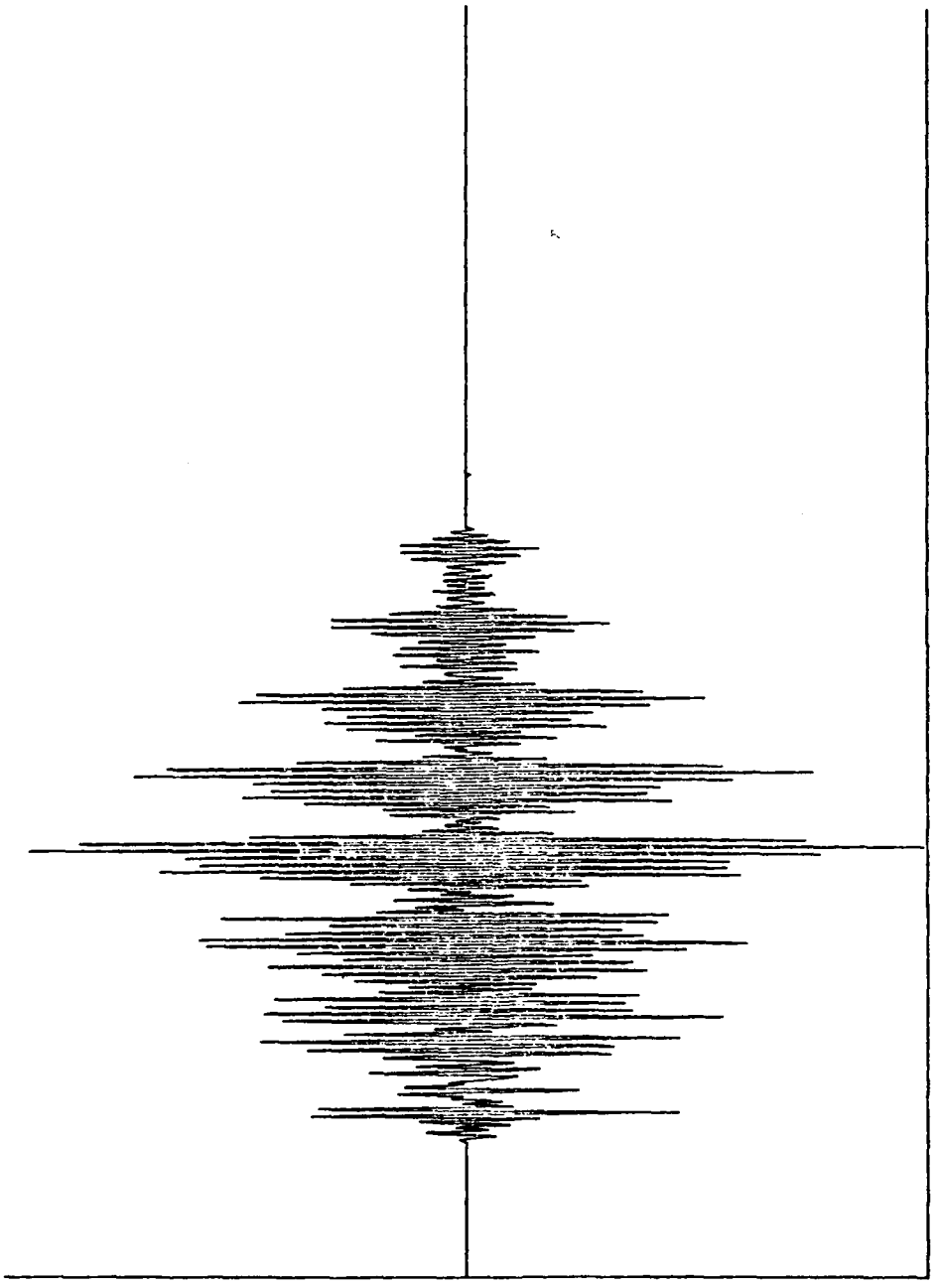

Figure 70. Typical Response

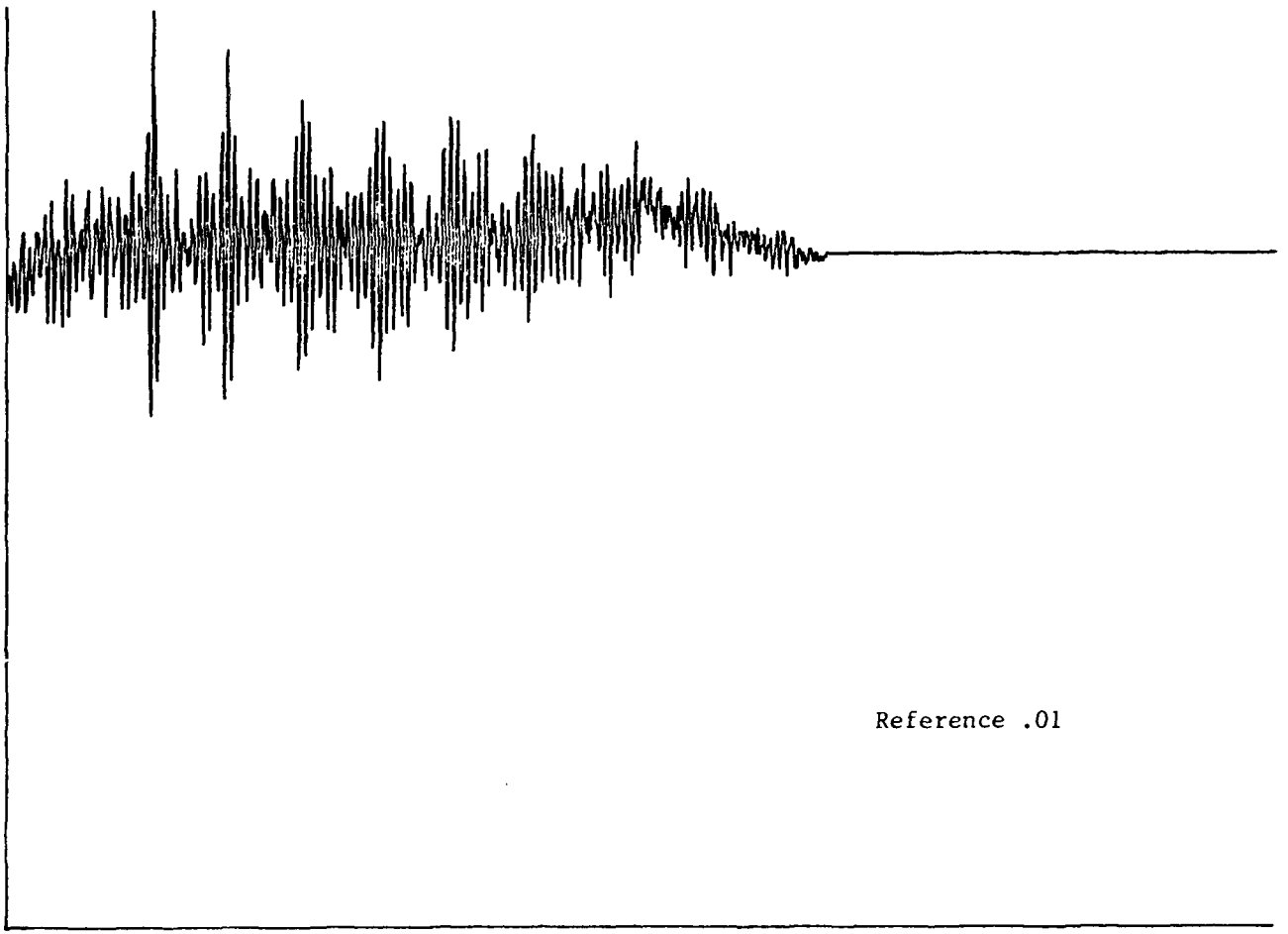


Figure 71. Signal Averaged Correlated Outputs with Averages Varied Through Two Averages

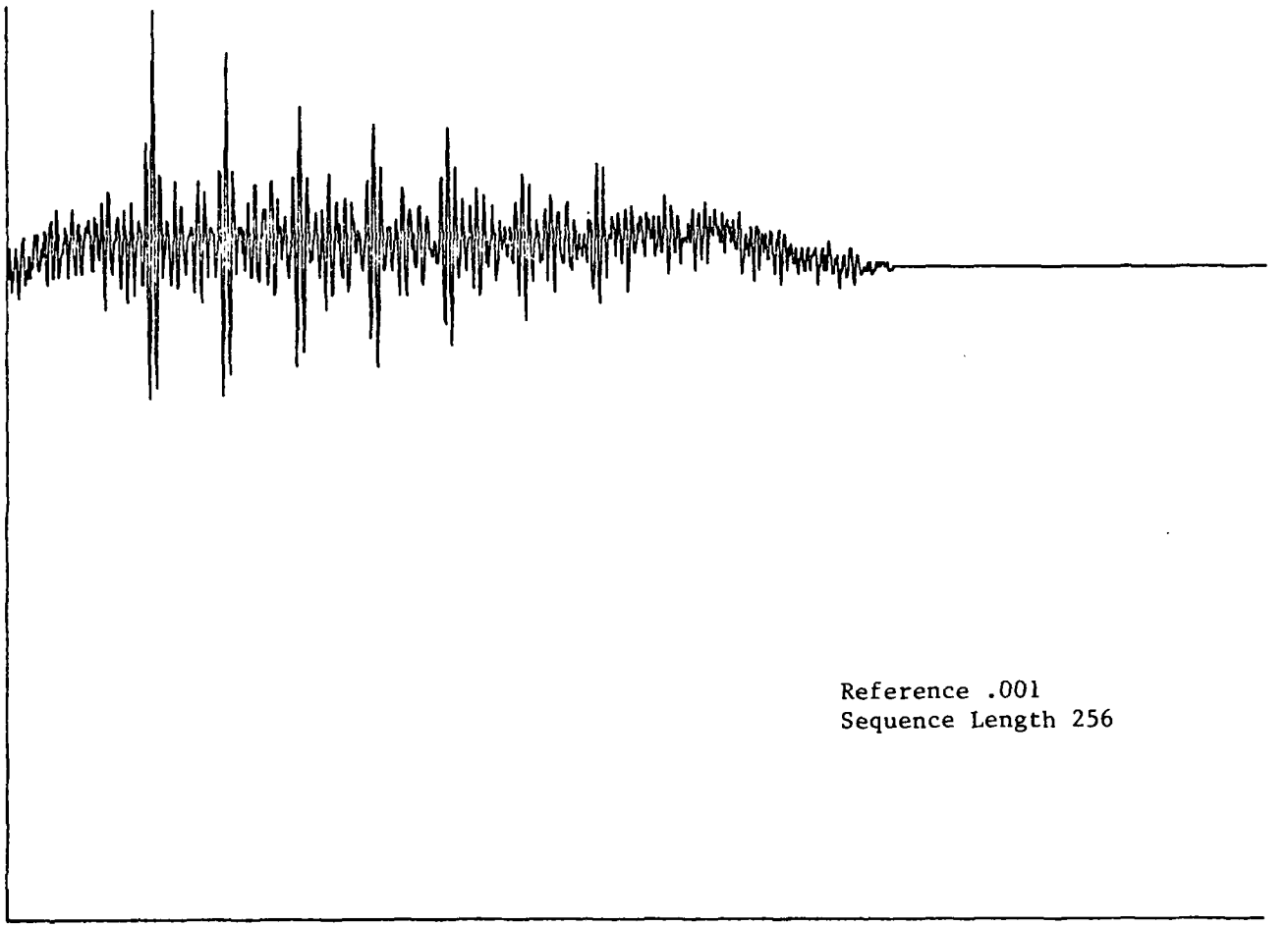


Figure 72. Signal Averaged Correlated Outputs with Averages Varied Through Four Averages

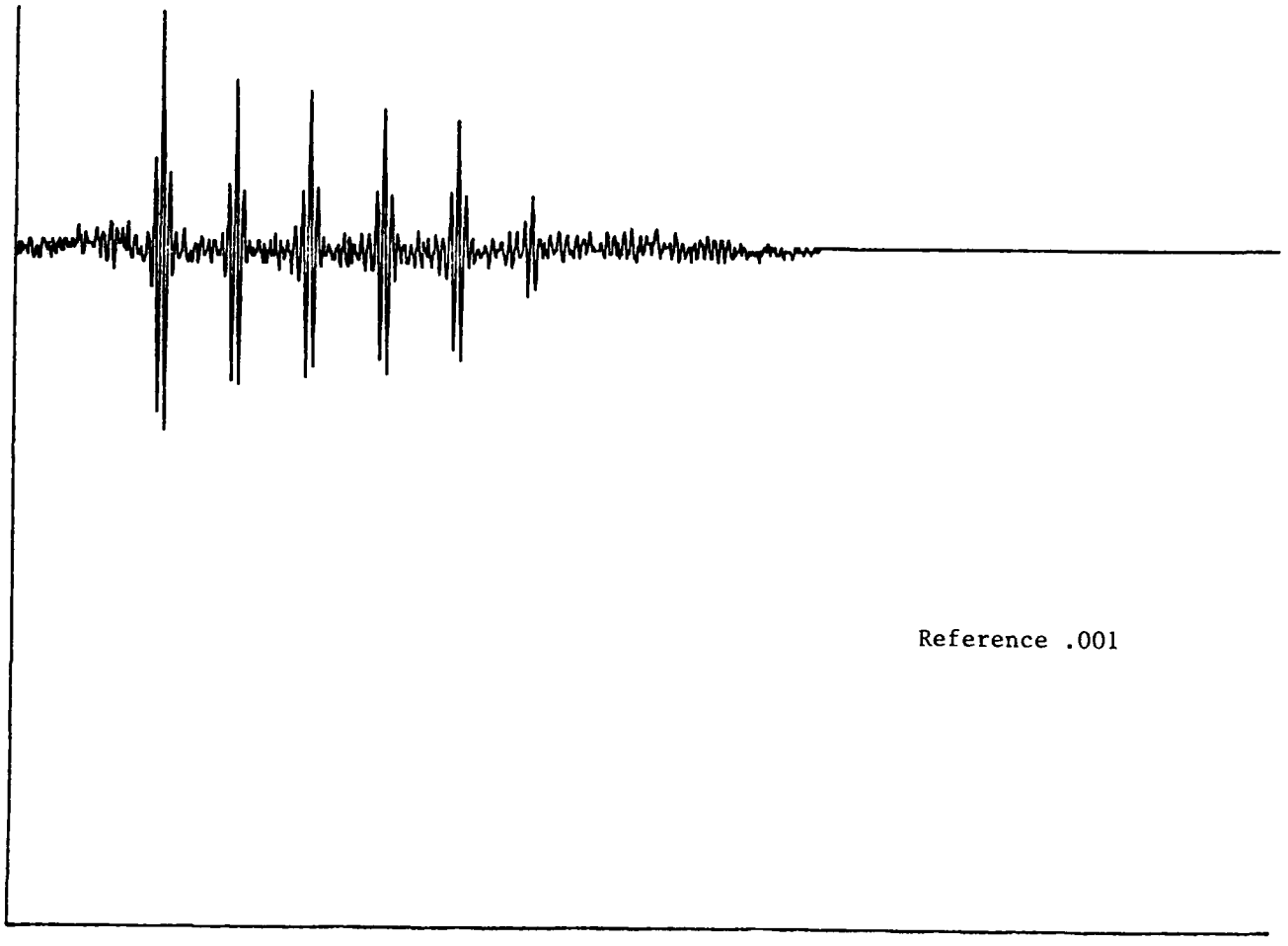


Figure 73. Signal Averaged Correlated Outputs with Averages Varied Through 16 Averages

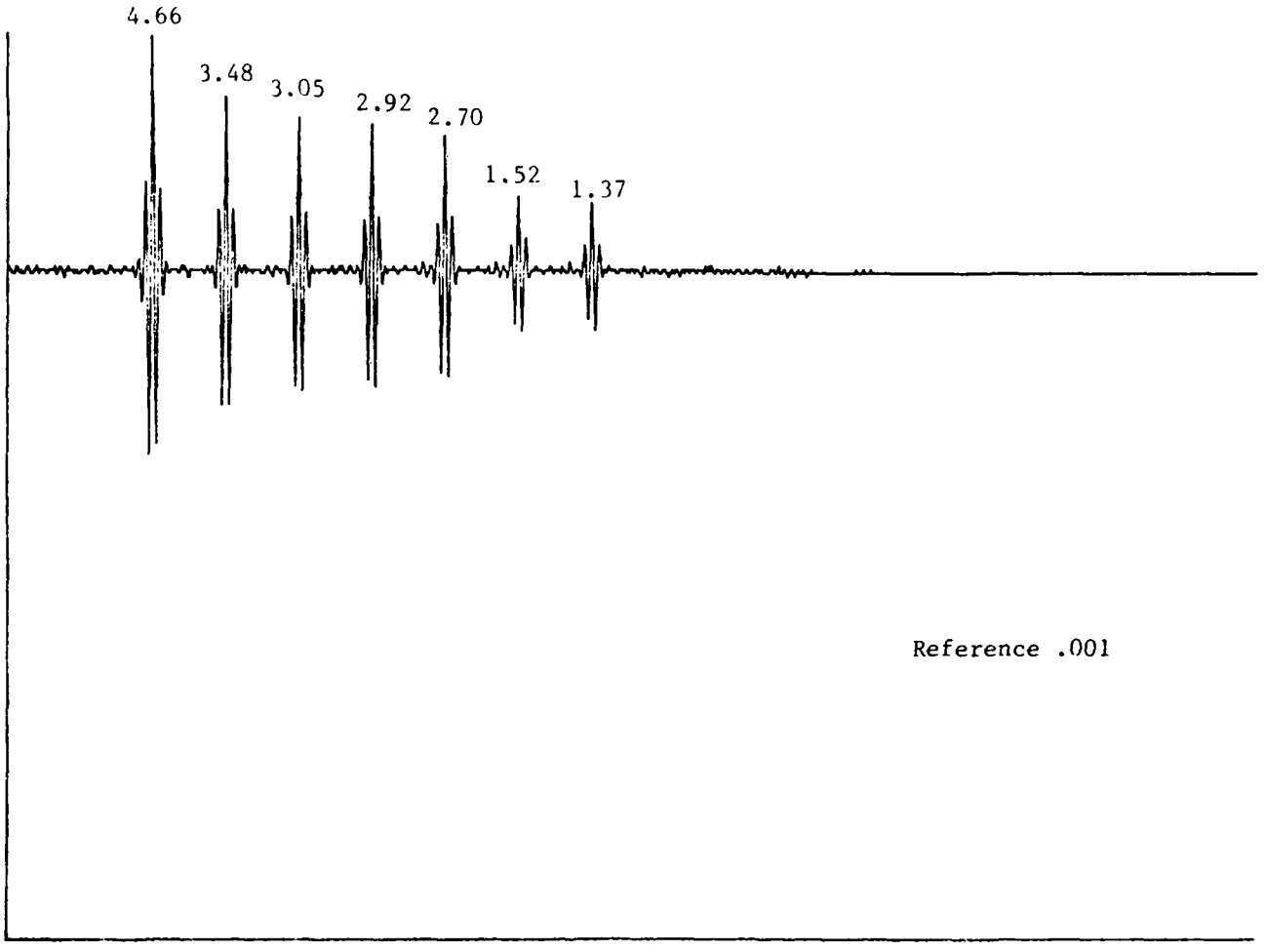


Figure 74. Signal Averaged Correlated Outputs with Averages Varied Through 256 Averages

To check linearity in the presence of additive Gaussian white noise, the model was designed to allow the introduction of noise to the y(nT) sequence after the convolution. Figure 75 shows the superposition of a Gaussian random noise sequence with the sequence shown in Figure 70. The resulting y(nT) sequence was 1-bit correlated and signal averaged 256 times, resulting in the correlated output of Figure 76.

The S/N of the y(nT) sequence of Figure 75 is ~1 and Figure 76 clearly shows increased linearity. The last two pulses are no longer visible with the signal looking similar to the original impulse response of Figure 69. To better quantify the linearity of the correlator model as a function of input S/N, the normalized outputs versus input amplitudes were computed for the first five returns shown in Figure 74 and 76. The results are shown in Figure 77.

If the 1-bit correlator model were perfectly linear, the response would be on the linear response line shown in Figure 77. But, as can be seen, the response is definitely nonlinear for large S/N and approaches linearity as the S/N becomes less than zero. It was believed from these results that a microprocessor controlled system could be constructed which would estimate the variance of the input noise from the sampled input at a given gain and use this information to control the gain compensation with stored empirically derived gain curves.

The computer model of the pseudorandom noise correlation system was very useful in evaluating system behavior. The model indicated that the initial approach to expanding the dynamic range without sacrificing speed would not be successful. Subsequent testing indicated that the nonlinearity introduced by the 1-bit correlator with S/N > 1 could be compensated by the microprocessor controller. It was further indicated that signal averaging would be necessary to reduce the signal-to-sidelobe ratio. No attempt was made to achieve any greater quantification from the model.

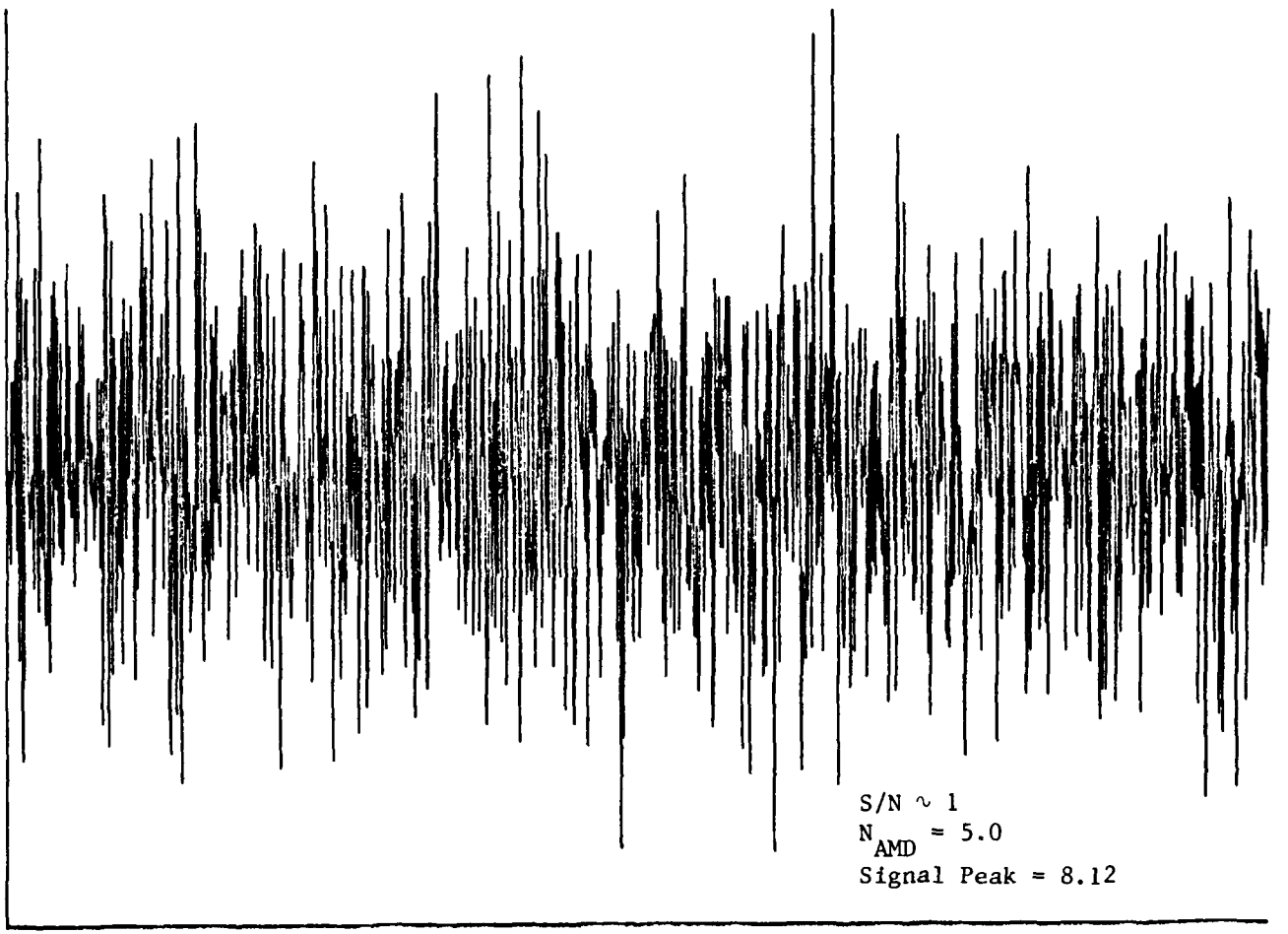


Figure 75. Superposition of a Gaussian Random Noise Sequence

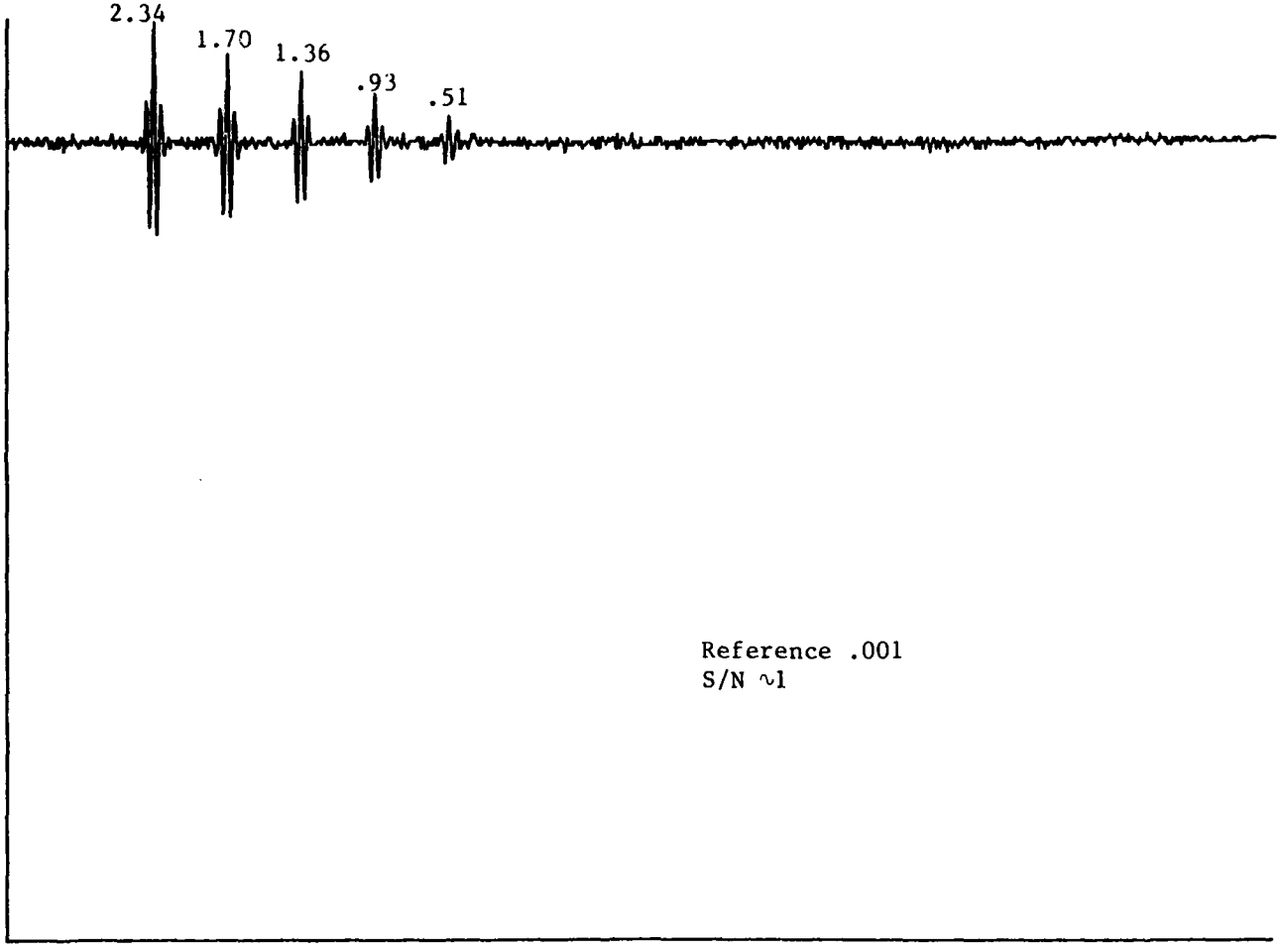


Figure 76. Correlated Output

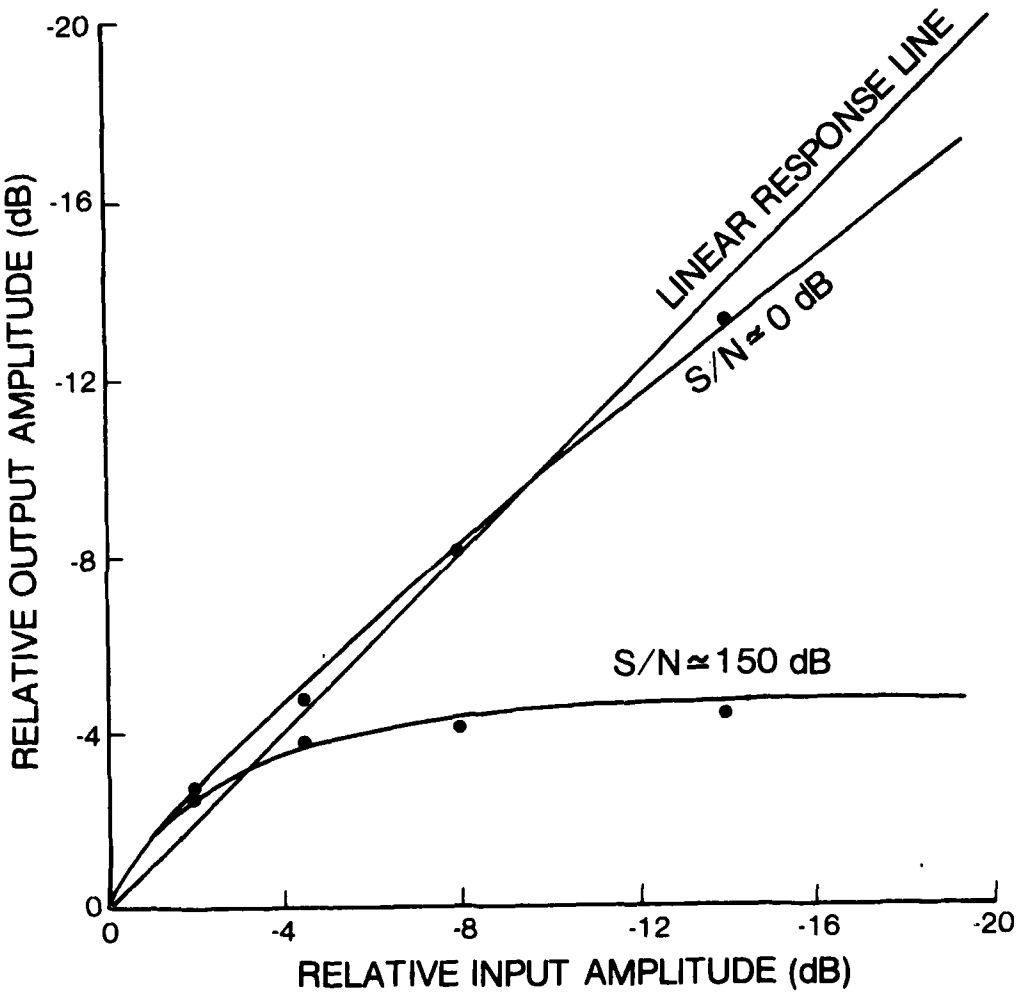


Figure 77. 1-Bit Correlator Model Linearity

## 3. SYSTEM DIAGRAM

The block diagram of the correlator system is shown in Figure 78. The system is designed for high speed digital sampling of the input waveform and high speed digital correlation on the complete sampled input waveform with the stored pseudorandom-binary sequence.

The front end of the correlation unit has selectable sample conversion rates of 60 MHz, 30 MHz, and 15 MHz. The digitally sampled input is stored by multiplexing high speed TTL random access memory. The sampling system can store up to 4096 points at each repetition. This will make the maximum sample period 34 μsec which corresponds to approximately 8 inches of longitudinal inspection in stainless steel.

The correlation system consists of a 1-bit wide, 512-bit long digital-to-analog correlator. The correlation process is achieved by the utilization of the TRW 64-bit correlator device, TDC1021J. The correlator processes each sampled data point at a 100 nanosecond rate. A 10 KHz pulse repetition rate (PRF) can be achieved with the proper selection of burst length, sample delay, and sample points.

### a. Digital Sampler and Signal Averager

One of the problems in the use of Pseudorandom-Binary-Signal One-Bit Correlation is the nonlinearity which occurs as the signal-to-noise ratio approaches one and the processed signal level exceeds the bit capacity of the system (saturate). It was planned to correct for this problem by installing a switching system which would convert operation to a conventional but very high speed digital sampler and signal averager as this condition was approached. Preliminary design was performed upon this sampler/signal averager as illustrated in Figure 79 through 81. Upon completion of the preliminary design, it was discovered that delivery times for some of the critical ECL integrated circuits and analog-to-digital converters exceeded 1 year (which made it impossible to construct, test, and

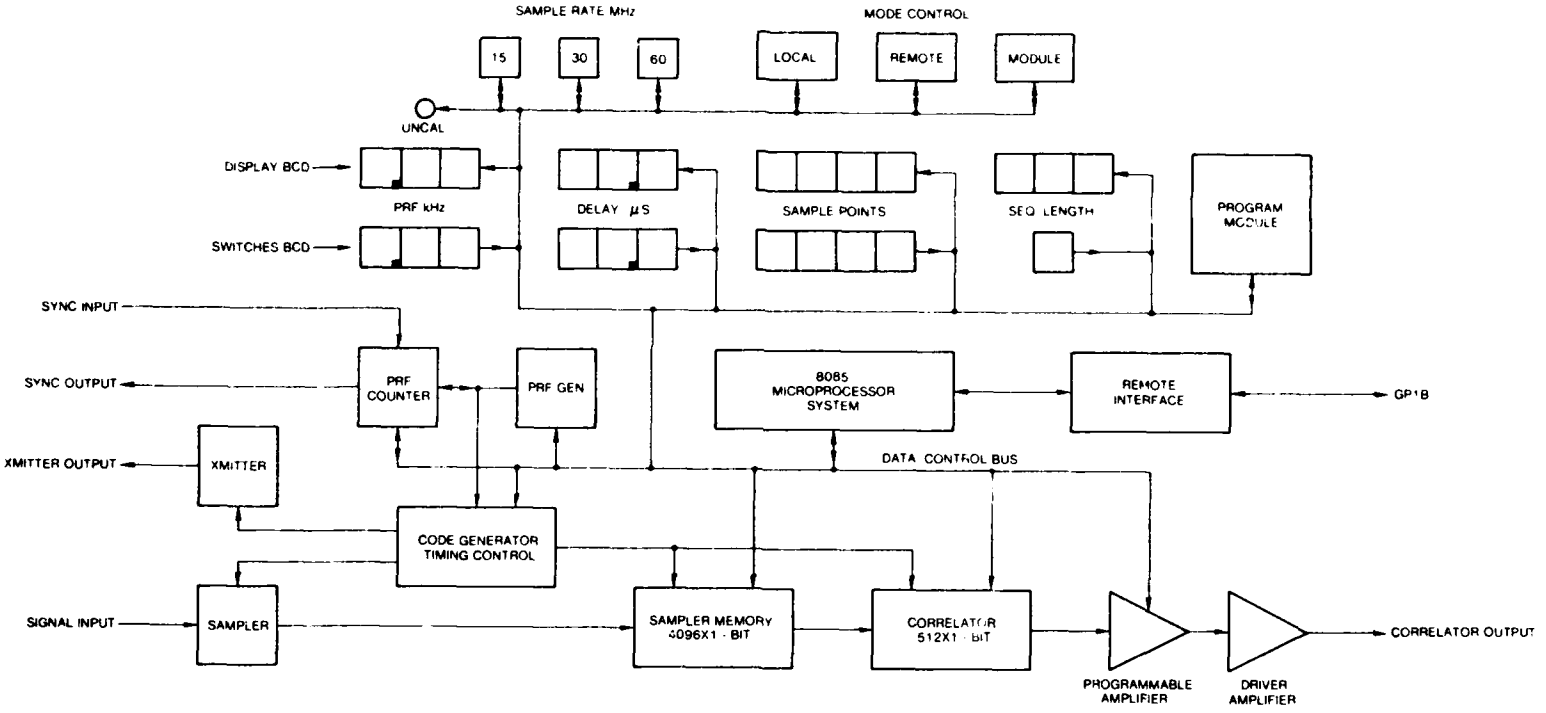


Figure 78. Block Diagram of the Pseudorandom-Binary-Signal Correlation System

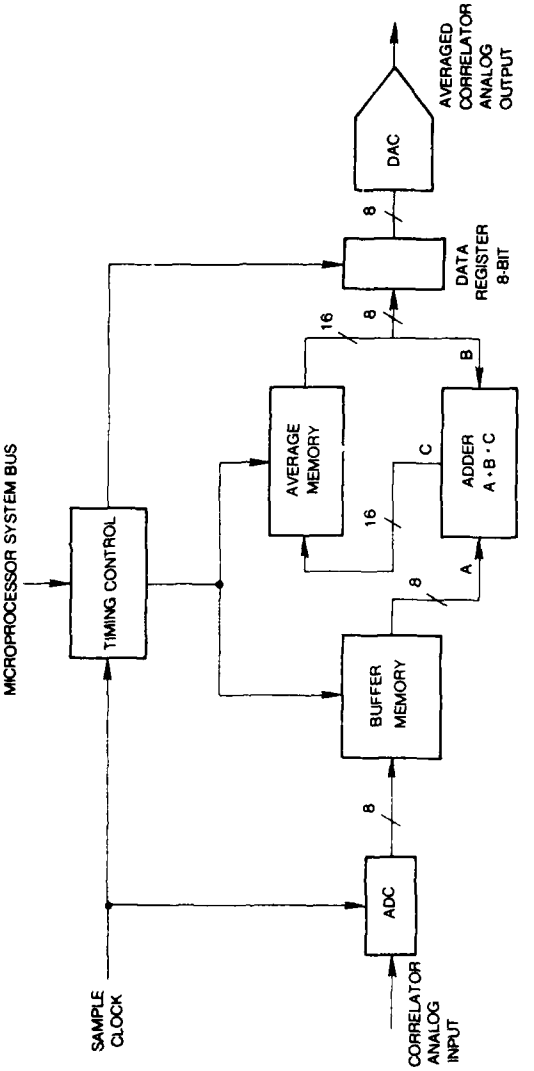


Figure 79. Block Diagram of Sampler Signal Averager

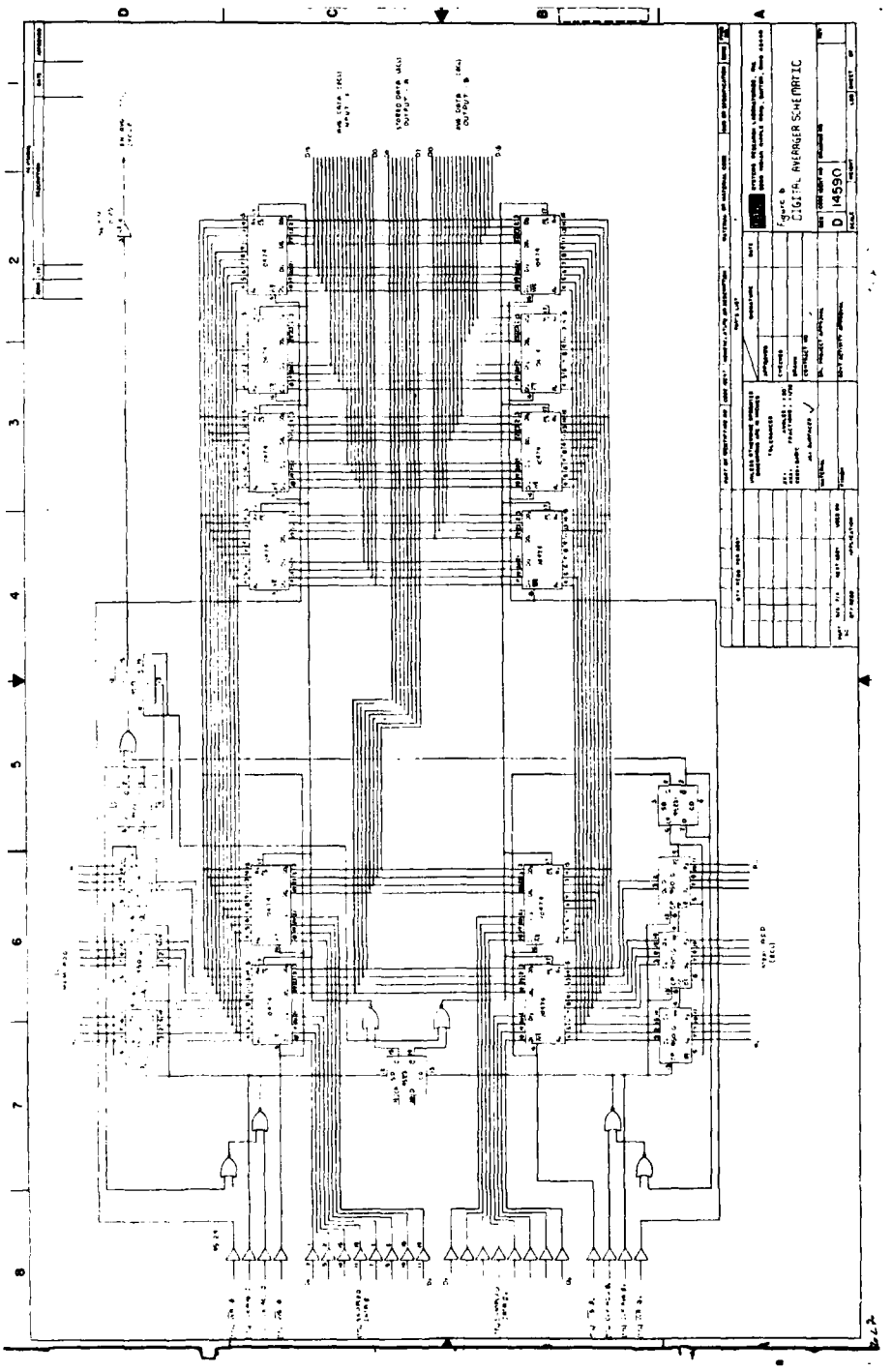


Figure 80. Digital Averager Schematic

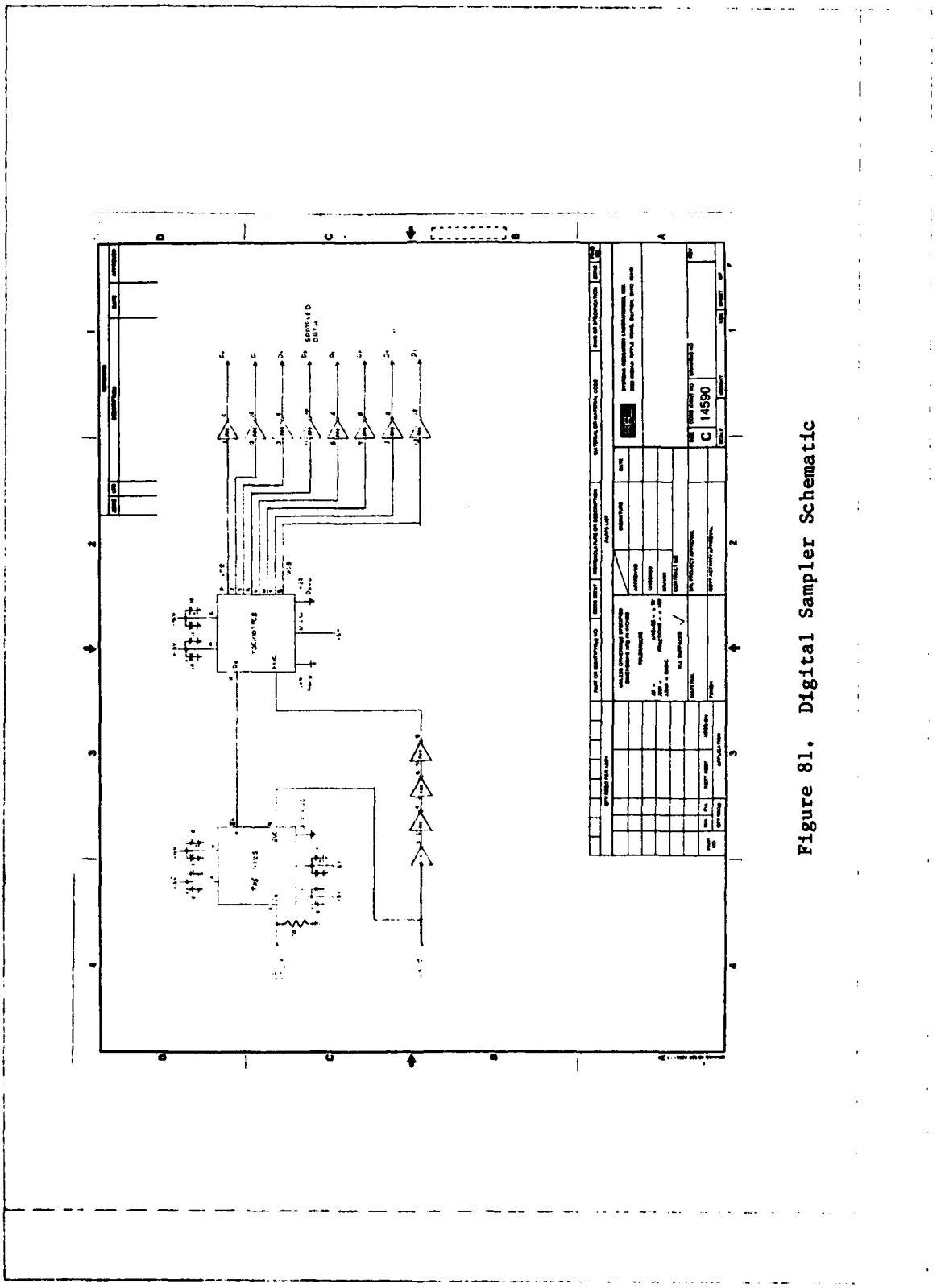

Figure 81. Digital Sampler Schematic

debug the system within the time frame of the program). Further work on the sampler/signal averager was terminated and full effort was redirected towards completion of the major goals of the program involving the pulser/receiver and the pseudorandom correlator circuits. In terms of the major objective of this program, which is to establish feasibility of the pseudorandom correlation process in a field type instrument, the lack of linearity at or near S/N ratios of one is not significant since such signals are handled quite well by conventional signal averagers.

## 4. FRONT PANEL CONTROLS AND DISPLAYS

The microprocessor-based correlator system allows all switches and controls on the front panel, or any command on the interface bus, to update the current selected value of any function. The program module increases the capabilities of the system by allowing all control functions to be stored and/or retrieved for any presystem programing applications. All displayed values of critical functions are the actual sampled value of the controlled parameters, and any system difficulties appear as an uncal condition or as error codes in the same display.

The correlator chassis and front panel are shown in Figure 82. All parameter controls are pushbutton rotary switches, and all mode selects are pushbutton illuminated momentary switches. The microprocessor scans the condition of each switch and updates each parameter according to the switch position. Each front panel control is described as follows:

PRF - Selects the transmitter pulse rate: 10 to 9990 Hz. Selects external input when switch setting reads 000 Hz.

Delay - Selects the delay of sample start from the end of the transmitted sequence: 0.1 to 99.9 microseconds in 0.1 microsecond steps.

Figure 82. Correlator Chassis

Signal Average - Inop.

Sample Points - Selects the number of data samples to be stored and correlated.

Data Output Rate - Inop.

Sequence Length - Selects the length of the pseudorandom-binary code to be transmitted: 64-bits to 512-bits in 64-bit steps.

Sample Rate - Selects the rate at which the pseudorandom-binary code is transmitted and the rate at which the samples are stored.

15 - Selects 15 MHz.

30 - Selects 30 MHz.

60 - Selects 60 MHz.

Mode Control - Selects the operational mode for the instrument.

Correlate - Selects the correlation mode of operation.

Sampler - Inop.

Cont. - Selects the continuous mode of correlation.

Single - Inop.

Reset - Inop.

Local - Selects instrument control via the front panel switches.

Remote - Selects instrument control via the IEEE-488 computer bus interface.

Module - Selects instrument control via the program module.

Program No. - Selects the module program number to control the instrument or to be programmed by the instrument.

Reset - Enters the control data from the module into the instruments program storage memory when operating in the module mode.

Alter - Allows for the control change of any front panel switch setting when operating in the module mode.

PRGM Store - Programs all front panel control switch settings into the program module at the location indicated by the program number switch when operating in the module mode.

Power - Turns on and off main power to the instrument.

5. MICROPROCESSOR SYSTEM

Reference Section III-3 of the Ultrasonic Pulser/Receiver System.

6. PROGRAM MODULE

Reference Section III-4 of the Ultrasonic Pulser/Receiver System.

7. PRF GENERATOR

Reference Section III-5 of the Ultrasonic Pulser/Receiver System.

8. PRF COUNTER

Reference Section III-6 of the Ultrasonic Pulser/Receiver System.

## 9. RECEIVER AND CLOCK GENERATOR

The schematic for the receiver and clock generator circuits is shown in Figure 83. The receiver performs the 1-bit analog-to-digital conversion on the input RF waveforms. A 300 MHz E.C.L. voltage comparator is used to perform the conversion, and an E.C.L. to T.T.L. converter is used to level shift the signals for system processing.

The input to the receiver, REC, is protected up to ±100 volts. The output, RDI, is connected to the input of a multiplexer circuit, shown in Figure 84 of the code generator, timing control, and transmitter schematic.

The clock generator circuits develop the various clock frequencies used in the system. The frequencies generated are 60 MHz, 40 MHz, 30 MHz, 15 MHz, and 10 MHz. The 60 MHz, 30 MHz, and 15 MHz frequency outputs, XSC, are selected by the microprocessor, Sample Clk Select, for the transmission of the pseudorandom-binary sequence and the input sampling rate. The system will sample and store the analog input, REC, at the same rate the sequence was transmitted. The 40 MHz frequency output, DC, is used to generate the sample delay. The range of the sample delay is from 00.1 μsec to 99.9 μsec, in 00.1 μsec increments. The maximum delay is limited by the front panel delay switches. The maximum delay would increase to 410 μsec with the addition of a higher order digital switch on the front panel. The 10 MHz frequency output, CCC, is used during the correlation process and when the pseudorandom-binary sequence is stored in the memory and correlator circuits. The system will correlate the sampled data at a 100 nanoseconds per bit rate. The XSC, DC, and CCC outputs are connected to the input of a multiplexer circuit, shown in Figure 84.

The various frequencies generated by the clock circuits are automatically synchronized to the rising edge of the internal or external PRF clock. The synchronization will expand the correlator's compatibility with other equipment.

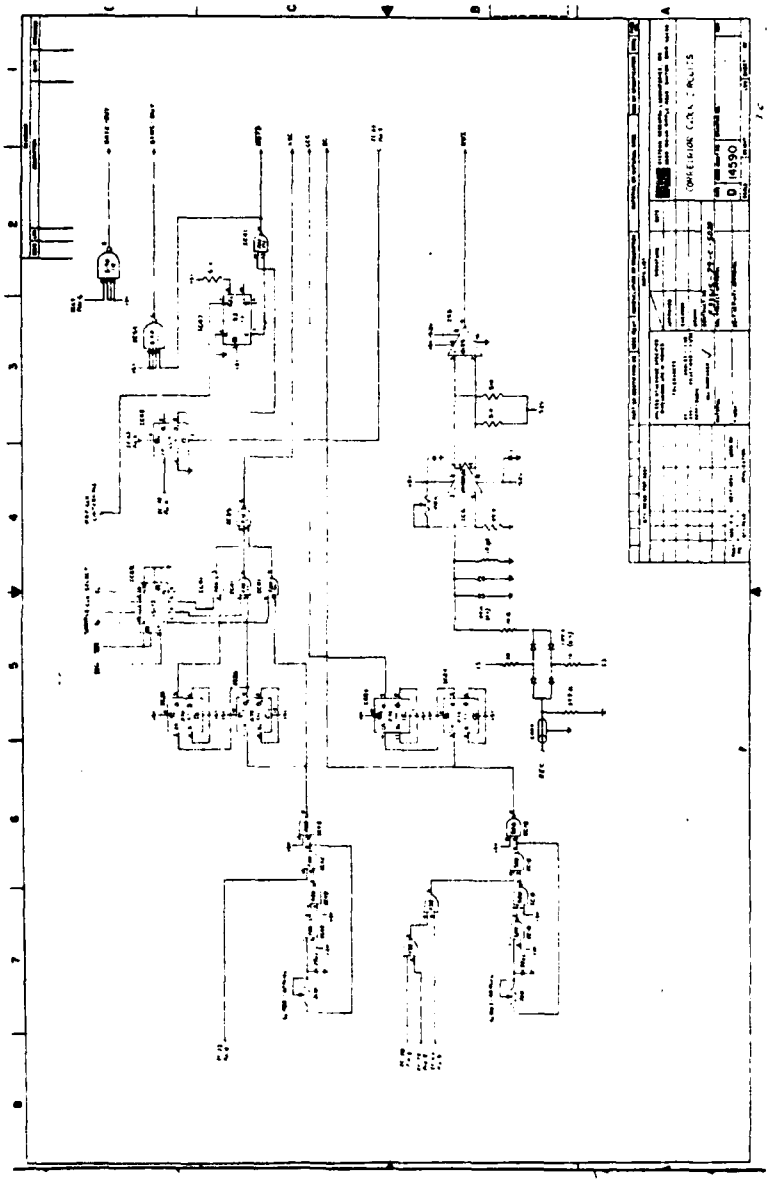

Figure 83. Receiver and Clock Generator Schematic

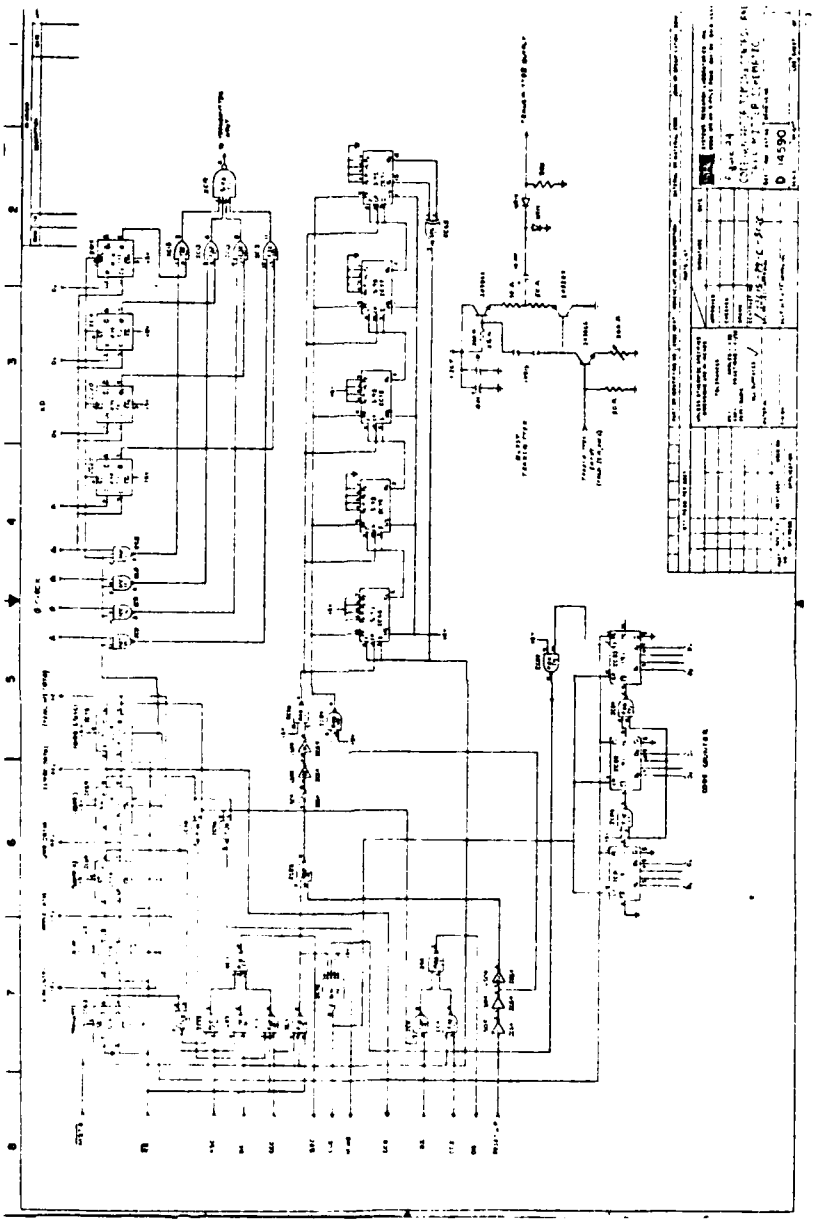

Figure 84. Code Generator, Timing Control, and Transmitter Schematic

10. SAMPLER

The high speed sampler circuits used for the sampling and storage of the digitized analog input, DI, are shown in Figure 85. The sampler circuits actually perform three system functions: (1) storage of input data for correlation, (2) storage of the pseudorandom-binary sequence for transmission, and (3) generation of the sample delay. The design utilizes a four-phase clock technique to sample and store data in four parallel channels. This reduces the operating frequency of each channel to one-fourth of the effective sampling frequency. The reduced channel frequency enabled the design to be accomplished utilizing commercially available T.T.L. integrated circuits and memory.

The data input, DI, to the sampler circuits is connected to the output of the multiplexer circuit shown in Figure 84 of the code generator, timing control, and transmitter schematic. The DI will be the digitized analog input data, DI, during the sampling cycle and the pseudorandom-binary sequence, and CCI, during the transmitter code store cycle.

The four-phase clock input, SEC, is connected to the output of the clock multiplexer circuit shown in Figure 84. The SEC frequency will be 60 MHz, 30 MZ, or 15 MHz during the transmit and sample cycles, 40 MHz during the delay cycle, and 10 MHz during the correlation and transmitter code store cycles. The cycles are sequential and are determined by an overflow condition of the memory address counters. The data input to the address counters are connected to the register circuits of the correlator system interface as shown in Figure 86. The data inputs to the counters are multiplexed and loaded into the counters at the end of each cycle.

The sample convert delay data inputs to the sampler circuit determine the hold-off period before the correlated data is made available at the output of the correlator system. The SE output is

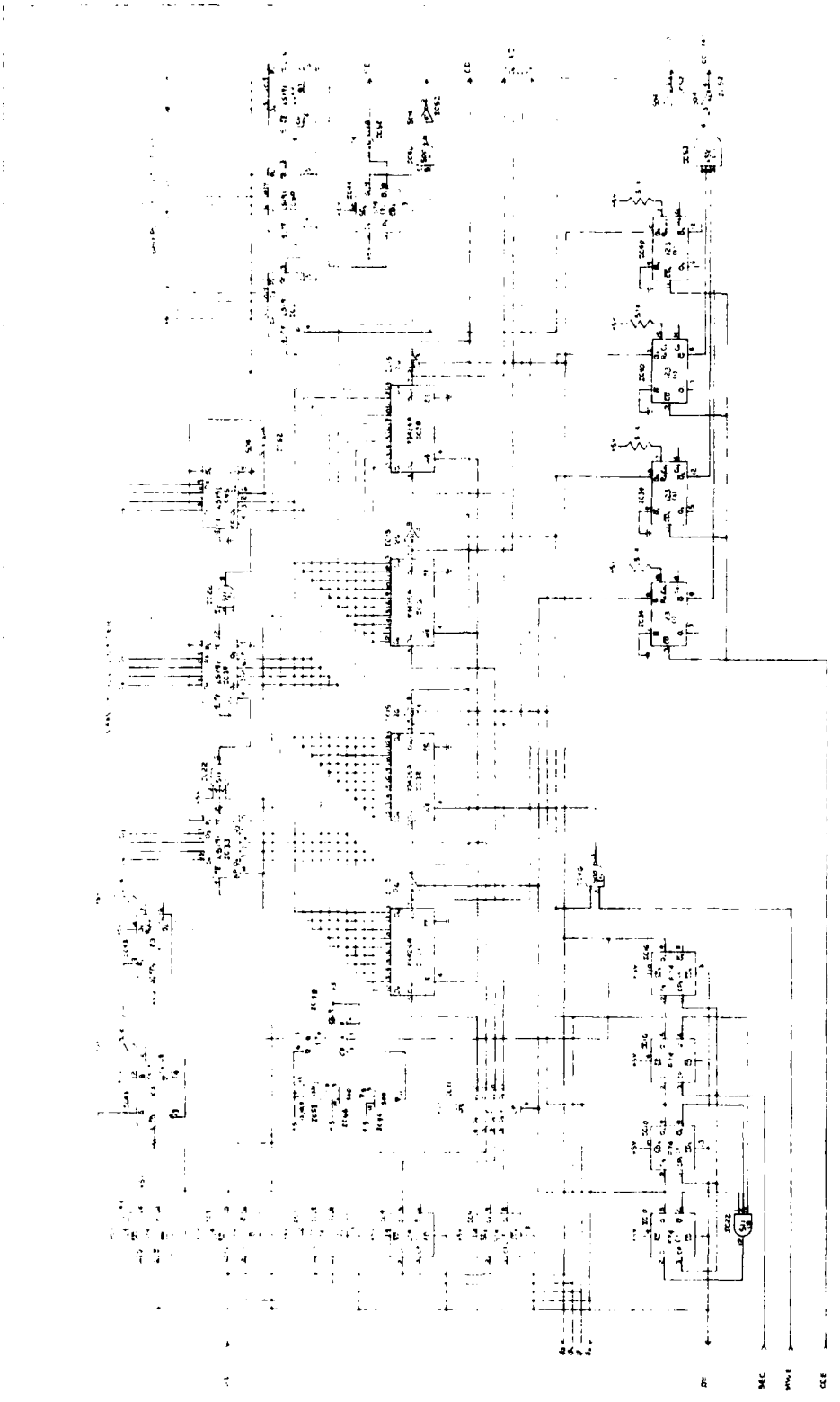

Figure 85. Sampler Schematic

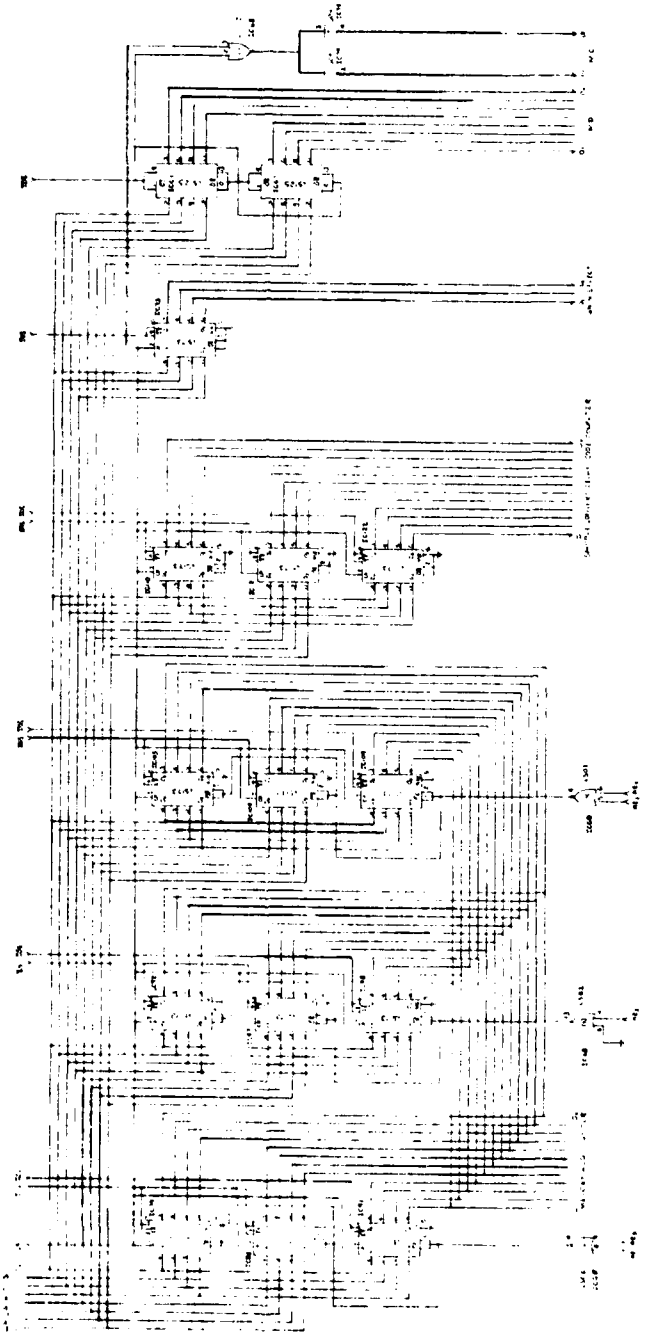

Figure 86. Correlator System Interface Schematic

connected to the enable input of the analog multiplexer, shown in Figure 87, of the correlator schematic. The hold-off period insures that there will be no correlated output until the correlation registers are completely filled with sampled data, thereby reducing the large DC offsets that may occur at the beginning of the correlation process. The SC is a synchronized clock output that may be used to trigger an analog-to-digital converter for the sampling of the output of the correlator.

The 1-bit sampled data output, CD, of the sampler memory is connected to the correlation circuits shown in Figure 87. The 4-bit transmitter code data output, XD, of the sampler memory is connected to the transmitter circuits shown in Figure 84.

## 11. CODE GENERATOR AND TIMING CONTROL

The pseudorandom-binary code generator and the system timing control circuits are shown in Figure 84. The pseudorandom-binary sequence is developed by a 20-bit long static shift register utilizing exclusive nor feedback. The sequence, CCI, is clocked out of the shift register at a 10 MHz rate and loaded into the correlators and stored in the sampler memory. The length of the sequence is selected, via the front panel, from 64 bits to 512 bits in 64-bit increments. The reset pulse, generated by the microprocessor system, is used to preset the shift registers to a predetermined start-up code.

The output of the timing sequencer, $AE_1$, $AE_2$, $AE_3$, $AE_4$, and $AE_5$, provides the enable pulses for each of the five cycles within the system. The timing sequencer is initiated on the following edge of a modified PRF clock pulse, $\overline{MBTD}$. The sequencer output state is changed at the advent of the reset pulse, $\overline{RE}$, which is generated by an overflow condition of the memory address counters, shown in Figure 85. The sequencer will stop at the end of the fifth cycle. The input PRF clock is disabled during cycling of the system to insure that the output of the correlator will not be affected by too high of a clock rate.

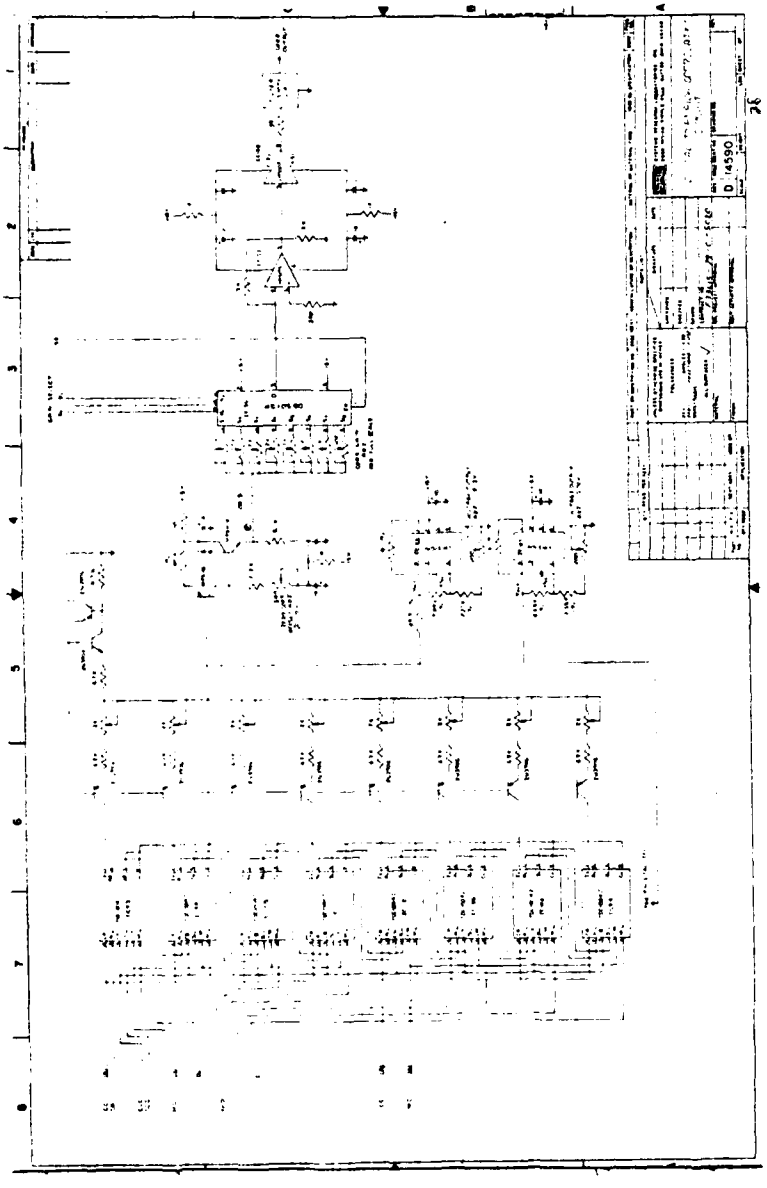

Figure 87. Correlator Schematic

The code counter data inputs determine the number of pseudorandom-binary code bits to be clocked into the correlators and the memory circuits. During the transmit cycle, the code, XD, is clocked out of the memory circuits and loaded into the transmitter shift registers. The code is then clocked out of the shift registers to the transmitter. The clock rate of the transmitter shift registers is four times the rate at which the data is being clocked out of the memory circuits.

12. CORRELATOR

The schematic for the correlation circuits is shown in Figure 87. The digital-to-analog correlation process is accomplished utilizing the TRW #TDC1004J, 64-bit correlator integrated circuit. The correlators contain a 64-bit data register, a 64-bit sequence register, and a 64-bit mask register. The output of the correlator is a current which is proportional to the combined sum of all the correlated bits between the data register and the sequence register. The mask registers, C, in the correlators are programmed by the microprocessor. Mask data, MD, is parallel clocked, MC(A) and MC(B), into each correlator via the microprocessor interface shown in Figure 86. The registers are programmed according to the selected pseudorandom-binary sequence length.

The correlator registers are connected in series to achieve a maximum correlation length of 512 bits. The sampled data, CD, is clocked, CC(A) and CC(B), into the data registers, A, and the pseudorandom-binary code, CCI, is clocked, CLC, into the sequence registers, B.

The full scale current output of each correlator is balanced by means of the adjustment potentiometers connected to the current input, IR, for each correlator. The outputs of the correlators are connected together and then connected to the positive voltage output supply

through a load resistor. A DC level shifter and amplifier is connected to the circuit at the correlator load resistor to eliminate the high DC offset and amplify the low level correlated signal.

The maximum correlation output current will decrease proportionally to the decrease in the maximum sequence length. To correct for this condition, a programmable gain amplifier was added to the output of the level shifter and amplifier circuit. The microprocessor selects a different precalibrated gain for each sequence length selected on the front panel. The output of the programmable gain amplifier is buffered to drive the 5 MHz, sharp cutoff, low pass filter, and any external load on the output of the system.

The limiting factor for the length of the transmitted pseudorandom-binary sequence is the number of correlators, #TDC1004J, used in the design. The sequence length may be increased in increments of 64 bits by adding additional correlators. A cost of $110 for each correlator was the limiting factor for eight correlators in this design. The correlation circuitry has been designed to allow for the expansion of the sequence length to 2048 bits.

## 13. TRANSMITTER

The pseudorandom-binary sequence transmitter schematic is shown in Figure 84. The transmitter develops the high voltage, high current pulse capabilities necessary to drive the transducer. The 200 ohm potentiometer is adjusted for an undistorted square wave pulse at the output.

## 14. CORRELATOR SYSTEM INTERFACE

The correlator system interface schematic is shown in Figure 86. The circuit provides an interface for program data between the microprocessor system and the function circuits of the correlator system. All function parameters of the system are programmed by the microprocessor and can be modified by software programming.

The data programmed into the registers enabled by control lines $AE_1$ and $AE_2$ determines the length of the pseudorandom-binary sequence to be transmitted and to be stored in memory, respectively. The data programmed into the registers enabled by control line $AE_3$ determines the length of the sample delay. The data programmed into the registers enabled by control lines $AE_4$ and $AE_5$ determines the number of sampled points to be stored in memory and the number of sampled points to be correlated, respectively. The microprocessor determines and loads the proper data into the system registers according to the front panel parameter settings. The data is loaded into the system only once, or until the front panel parameters are changed, to increase the speed of the correlation process.

15. FRONT PANEL INTERFACE

The front panel interface schematic shown in Figures 88 through 91 have been designed to interface directly to the controlling microprocessor bus system. All front panel switches and displays are accessed as input/output (I/O) devices. The switches and displays are assigned specific addressing codes according to their group functions. Reference Section III-19 for details on hardware operation.

16. REMOTE INTERFACE

Reference Section III-21 of the Ultrasonic Pulser/Receiver System.

17. EVALUATION

The correlator system has been evaluated to show: (1) the effect of certain system parameter changes on the correlated output, (2) high noise signal detection capabilities, and (3) flaw detection capabilities. This evaluation is limited and only involves those areas necessary to show compliance with the program requirements. A more indepth evaluation will be required to determine the full capabilities and specifications of the system.

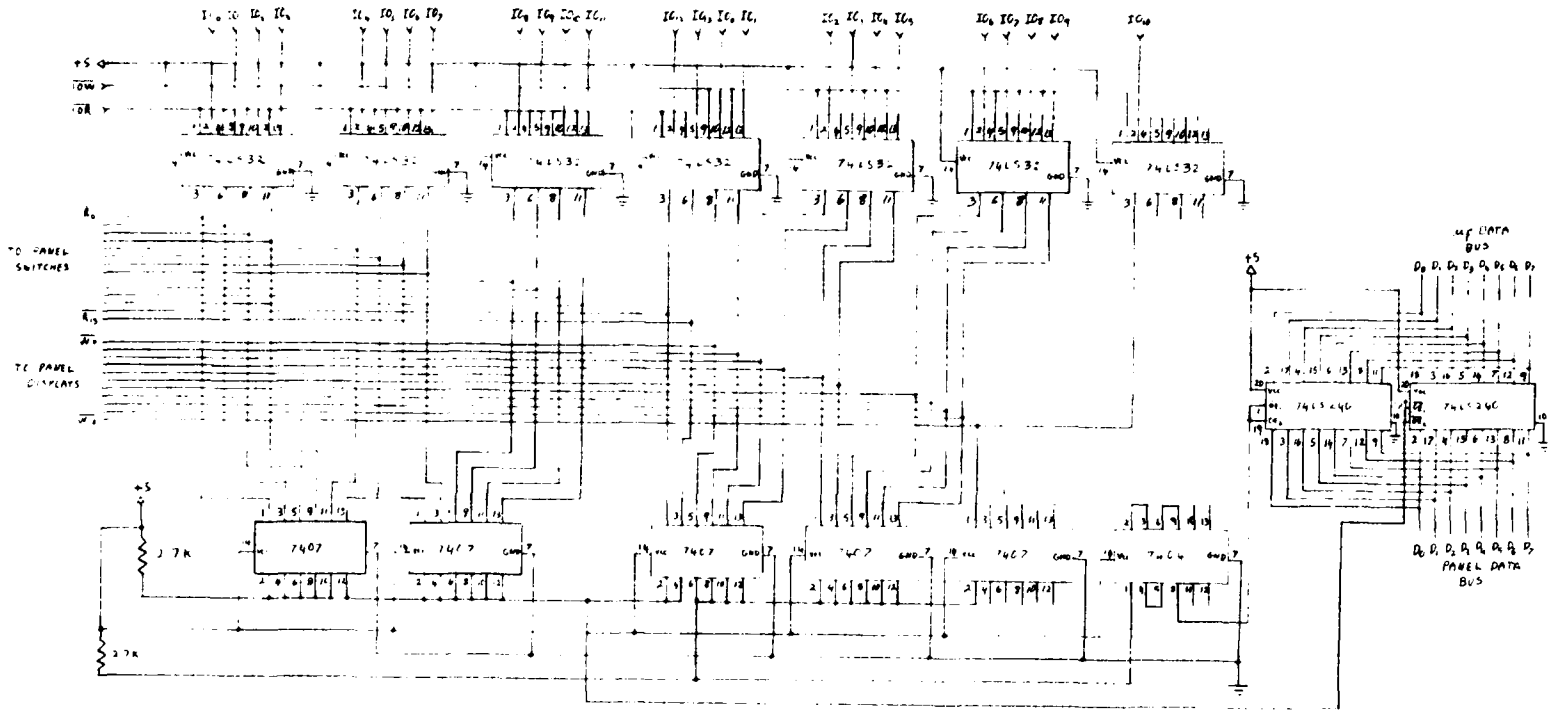


Figure 88. Front Panel Interface Schematic

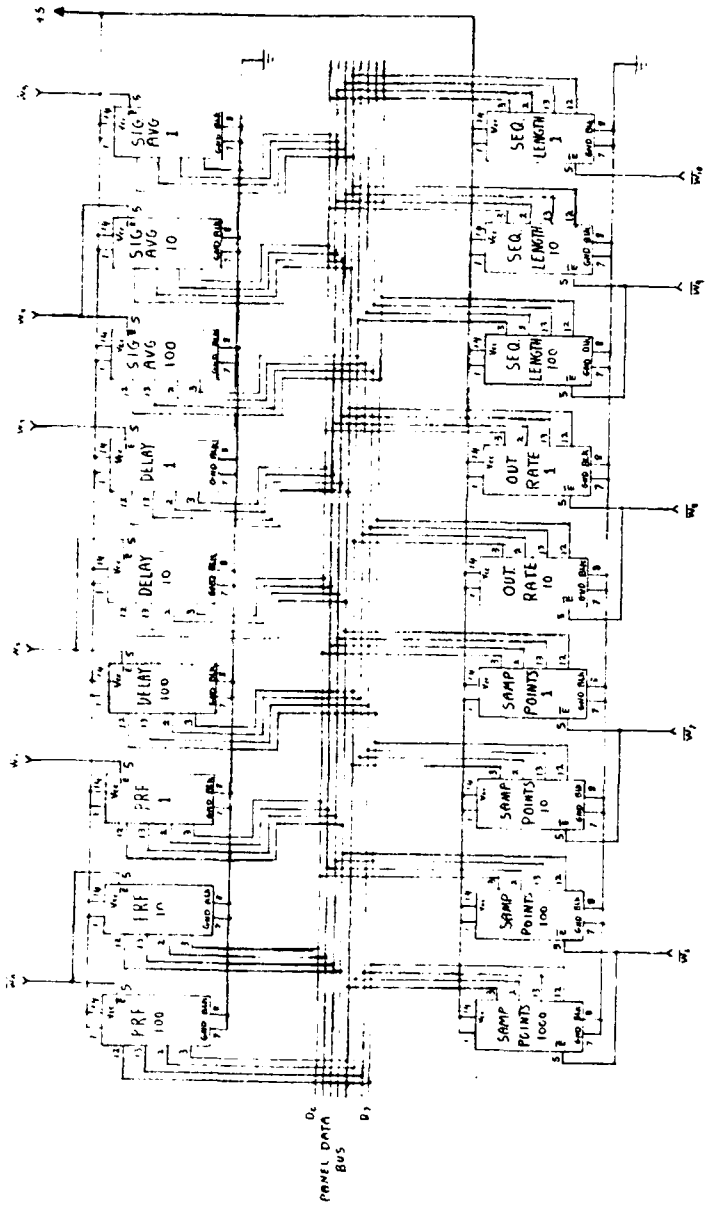


Figure 89. Front Panel Display Schematic

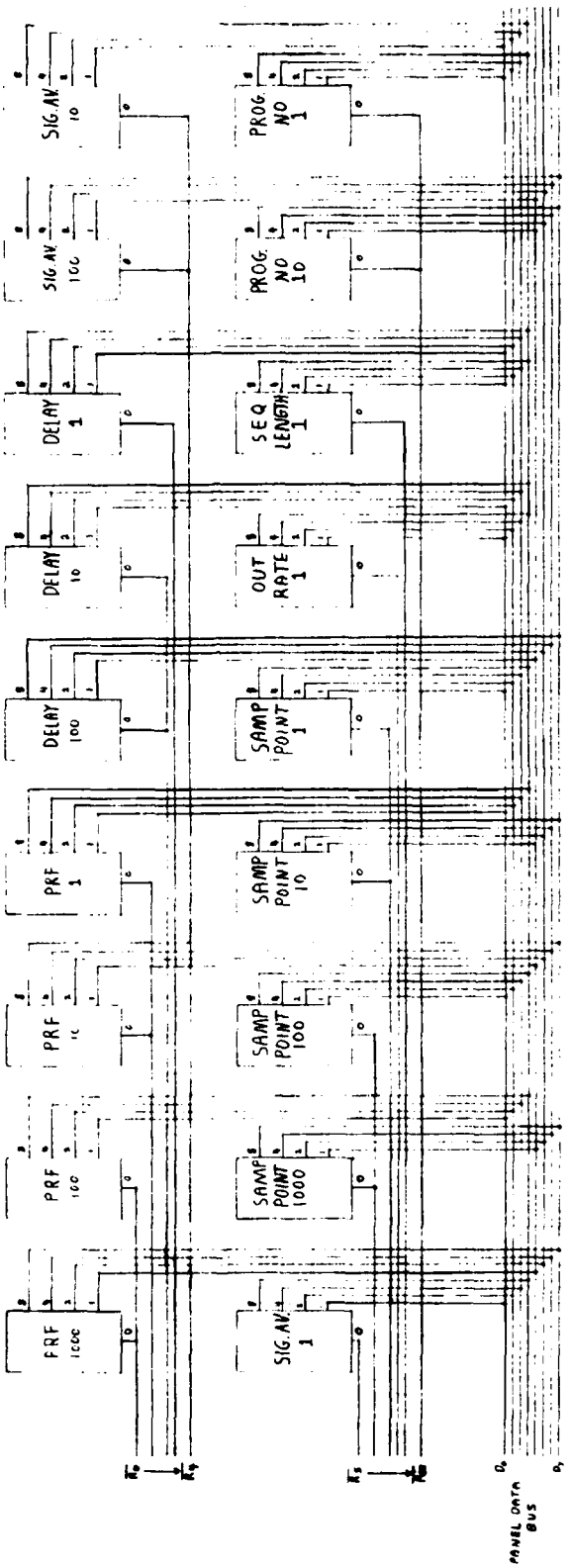


Figure 90. Front Panel Switch Schematic

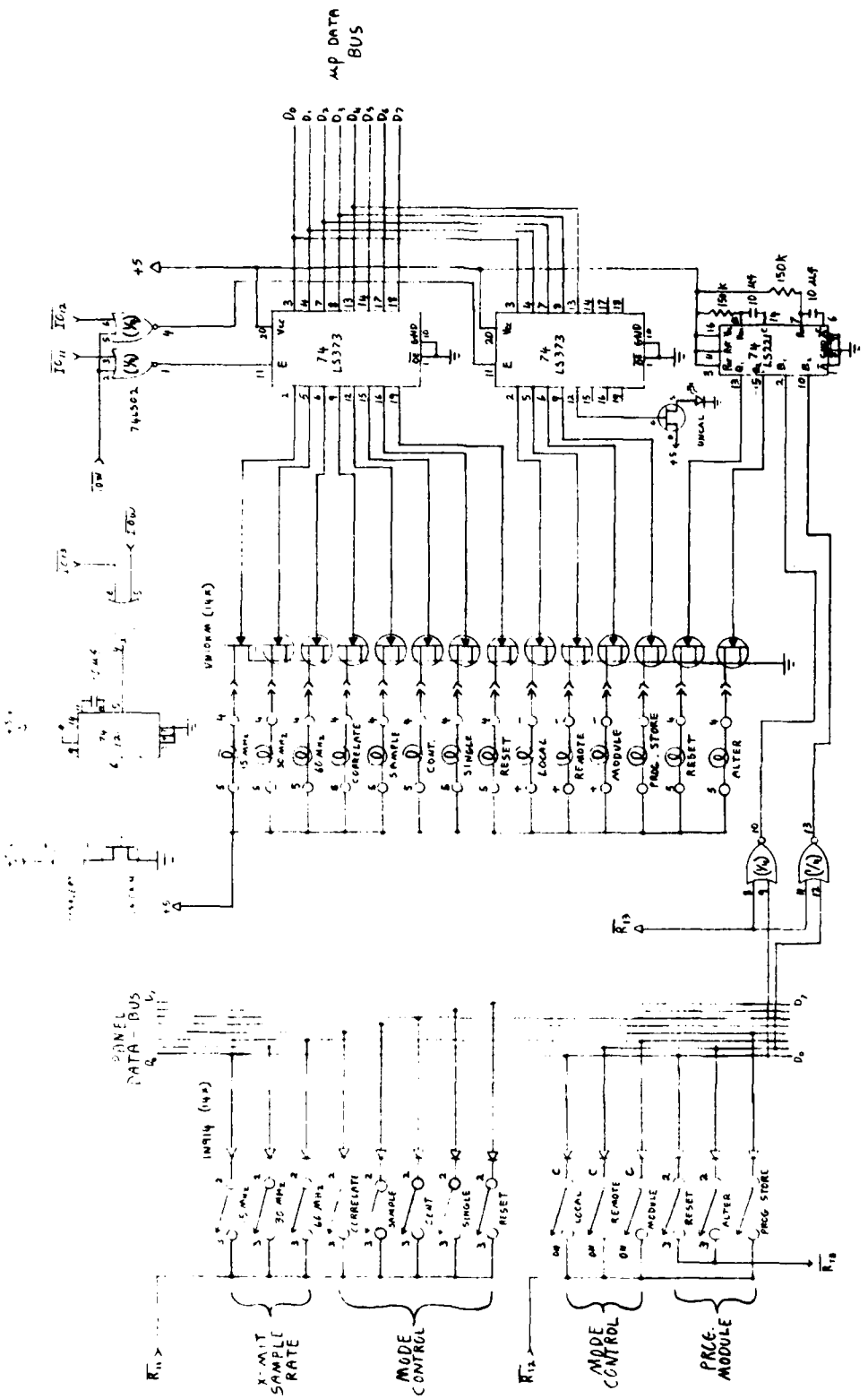


Figure 91. Front Panel Mode Control Schematic

The block diagram of the correlator evaluation system is shown in Figure 92. The pulser/receiver, developed under this program, was used as the input correlator amplifier and interface. The Tektronix mainframe, #7623A, with the sweep sampler, #7514, were used as a variable sweep delay sample and hold for the output of the correlator. The LSI-11 computer system converted the sampled analog output from the sweep sampler to digital information for signal processing. The DAC output from the LSI-11 provided the incremental sweep delay control to the sweep sampler. The parameters such as the number of signal averages and the number of sample points were entered into the system through the Lear Siegler ADM-3 serial CRT/terminal. The graphic evaluation results were viewed on the CRT/terminal before a hard copy was made on the Hewlett-Packard plotter #7225A.

The correlated output waveforms will not appear as real-time but, in effect, pseudo-real-time. This is due to the difference in the input sampling rates of 15 MHz, 30 MHz, or 60 MHz, and the fixed output correlation rate of 10 MHz. The labeling on the time axis of the evaluation plots reflect the actual period of the correlated output. The time axis shown is converted to real time by multiplying the time period by the correlator output rate and then dividing the result by the input sampling rate.

The effects of signal averaging on the correlated output is shown in Figure 93 through 96. An immersion type transducer was aligned to the front surface of the test sample and the signals were transmitted and received in the pulse-echo mode. The input signals to the correlator were adjusted for the highest, unsaturated output. The plots show the results of averaging 0, 100, 500, and 1000 times. The settings for the evaluation plots, shown in Figures 97 through 100, are similar to the preceding settings except that the input signals to the correlator were attenuated to produce a higher degree of noise at the output. The plots show the results of averaging 0, 100, 500, and 1000 times.

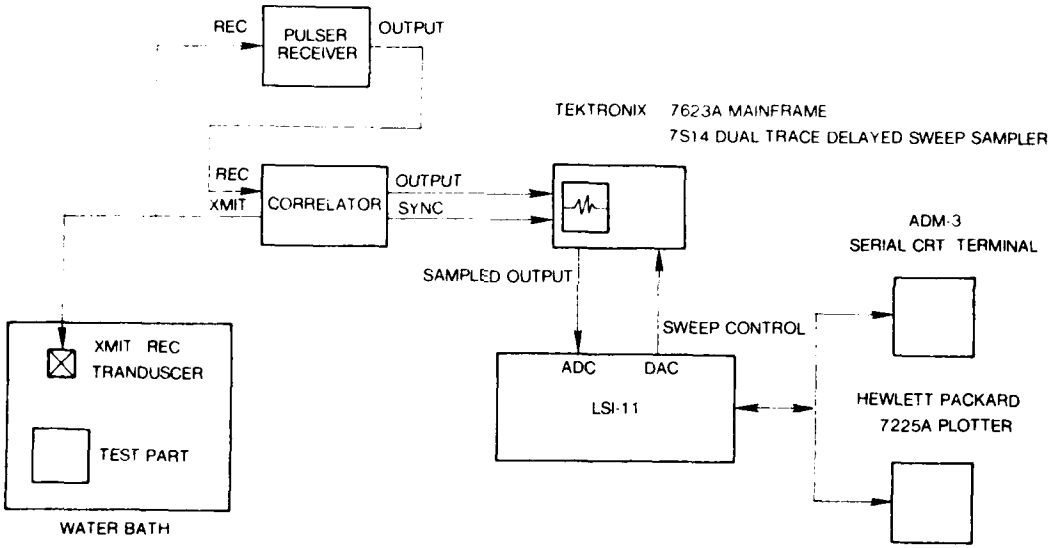


Figure 92. Block Diagram of the Correlator Evaluation System

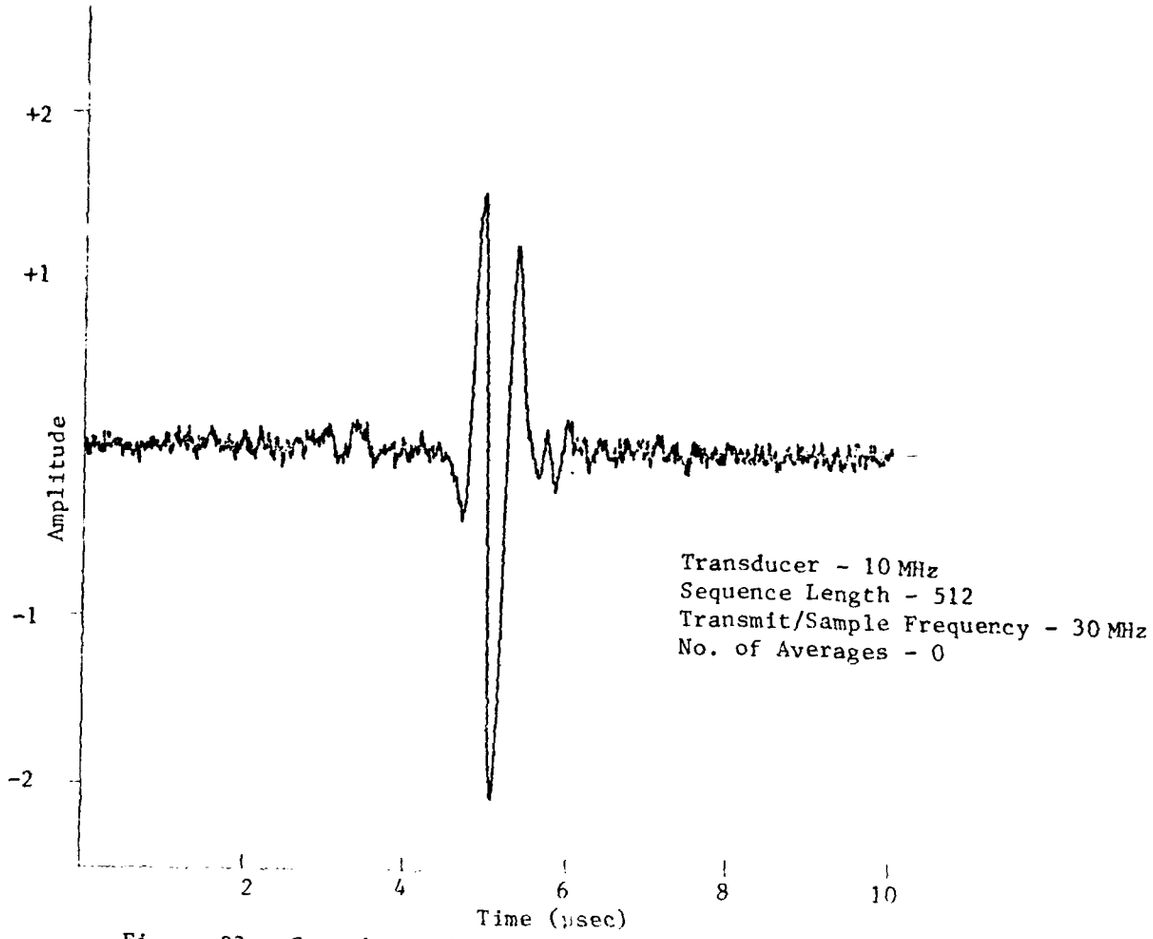


Figure 93. Correlator Signal Average Evaluation Plot

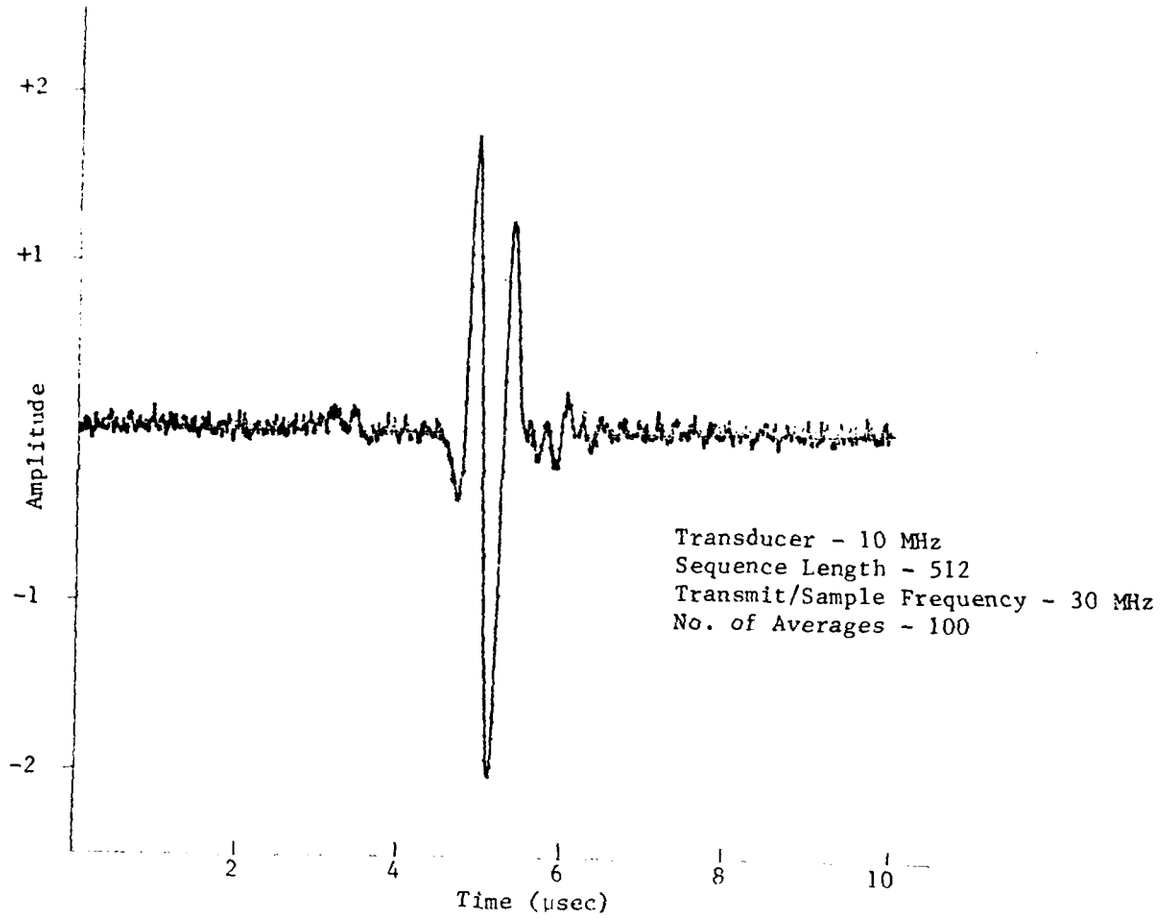


Figure 94. Correlator Signal Average Evaluation Plot

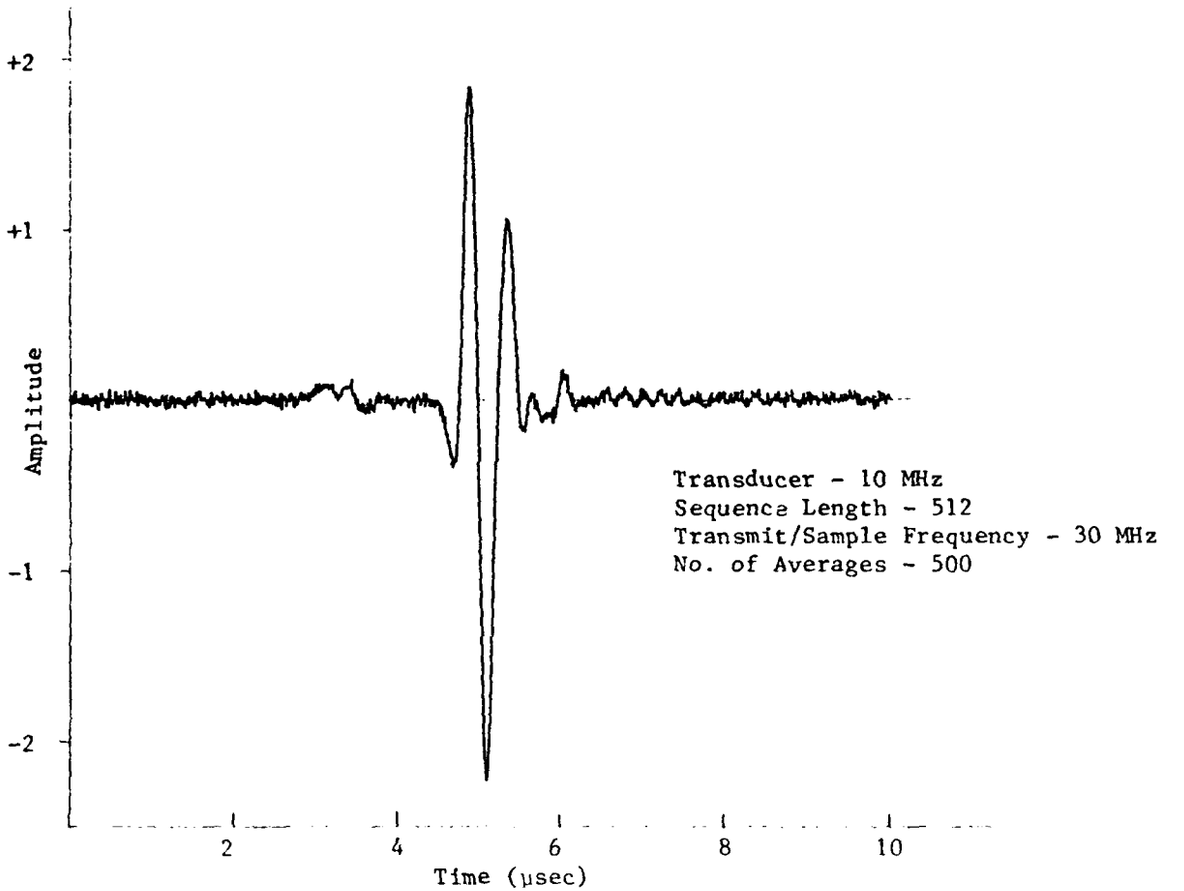


Figure 95. Correlator Signal Average Evaluation Plot

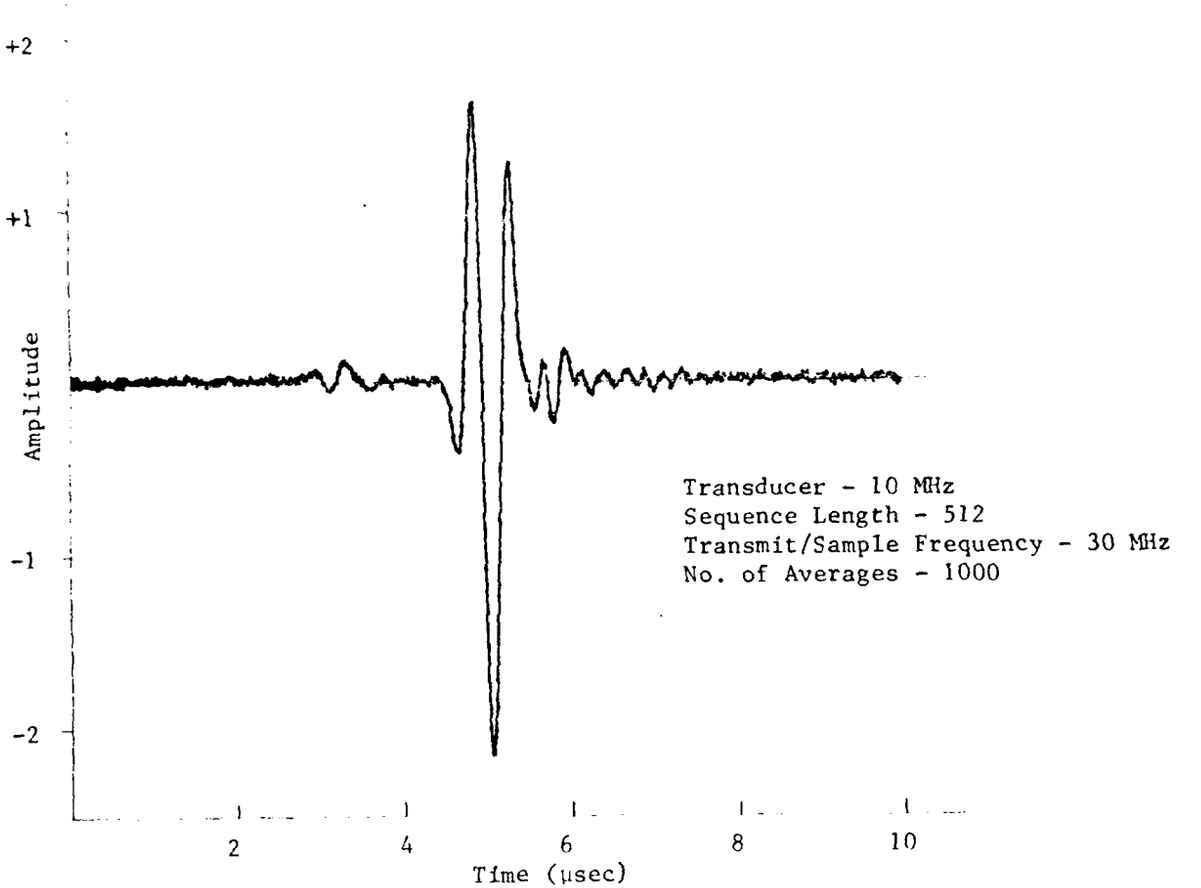


Figure 96. Correlator Signal Average Evaluation Plot

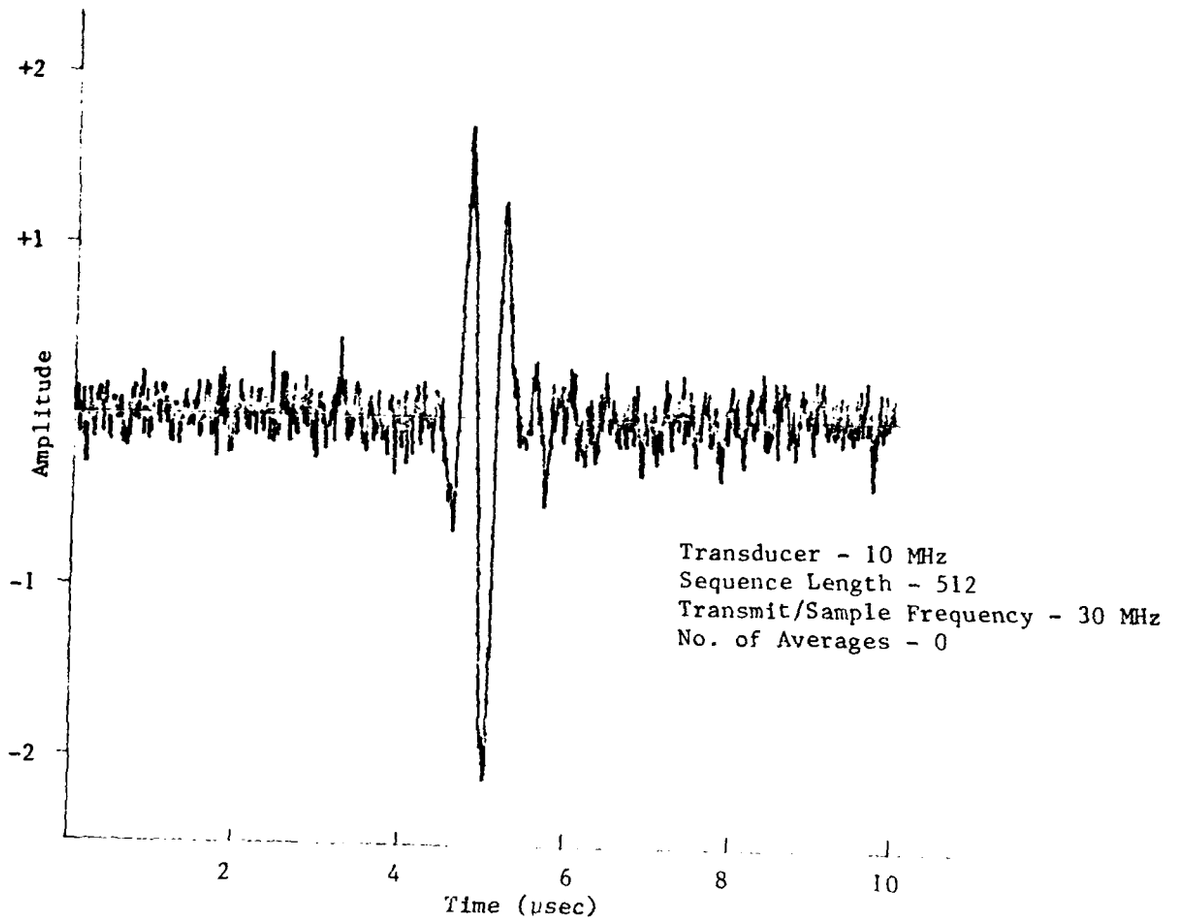


Figure 97. Correlator Signal Average Evaluation Plot

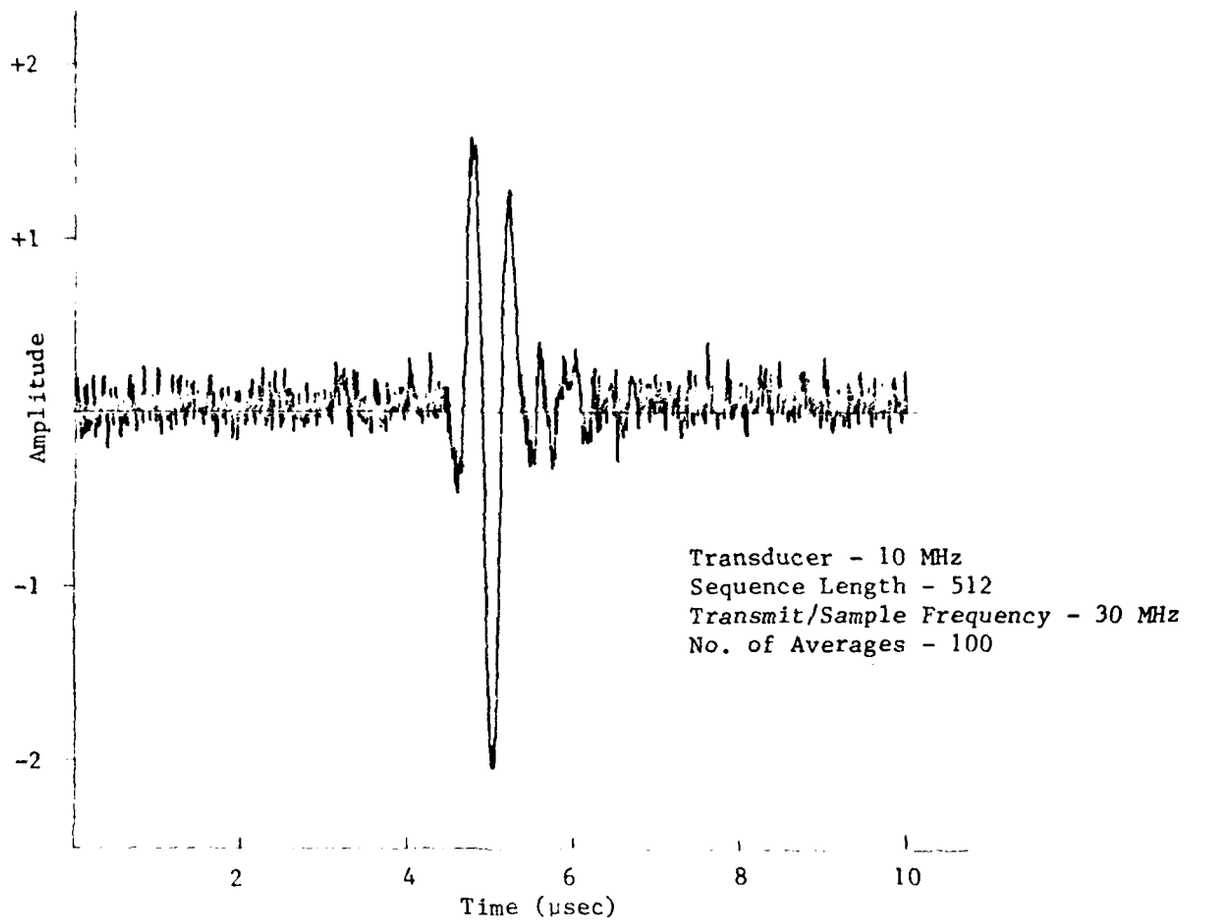


Figure 98. Correlator Signal Average Evaluation Plot

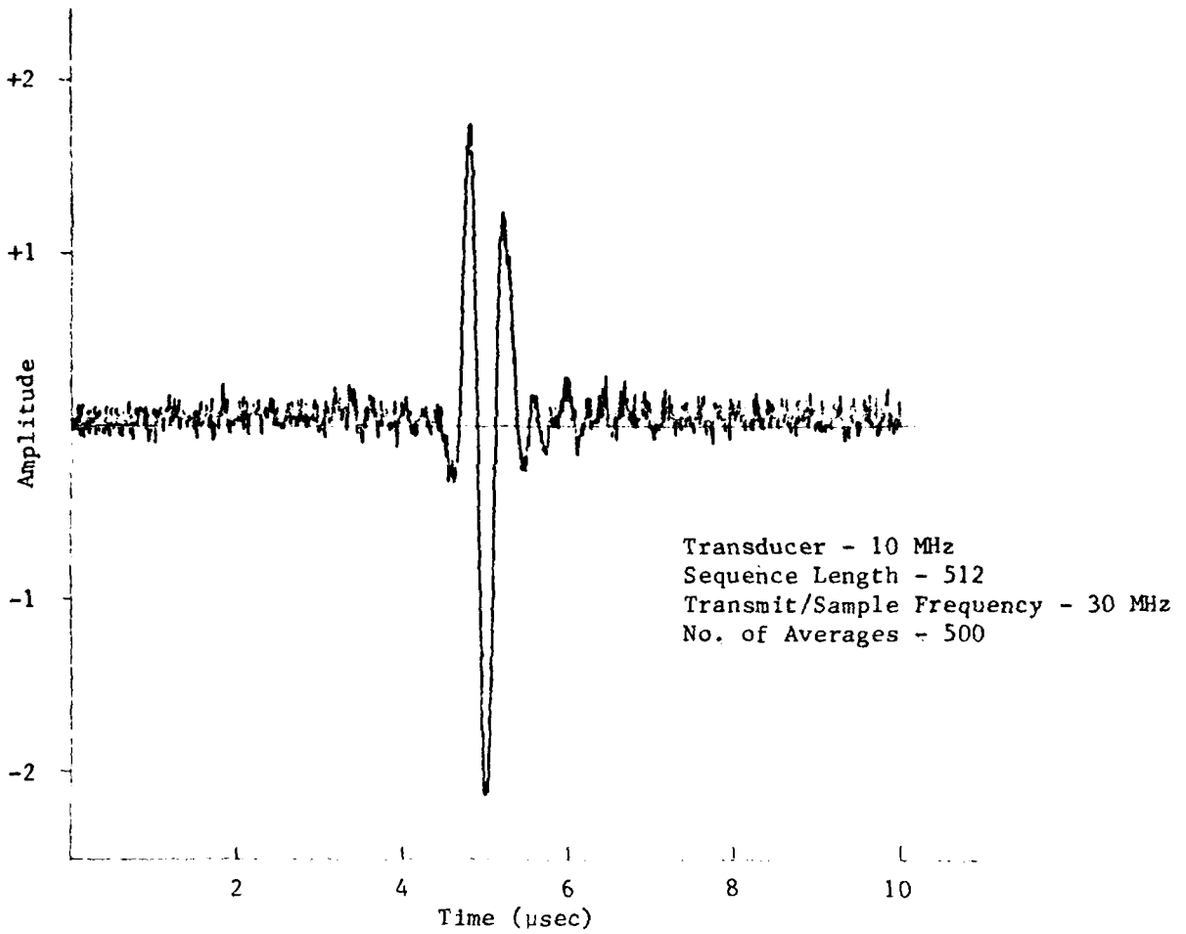


Figure 99. Correlator Signal Average Evaluation Plot

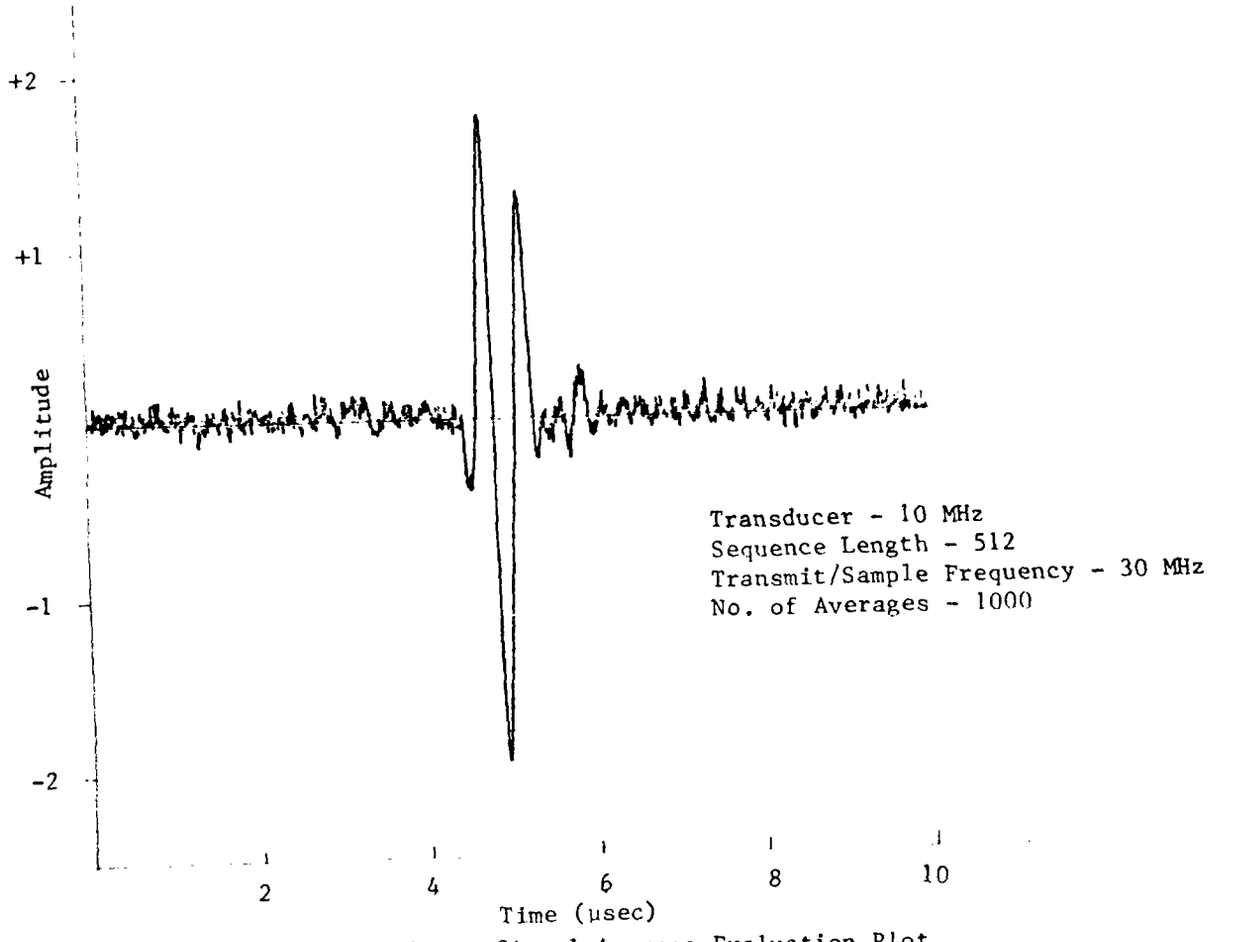


Figure 100. Correlator Signal Average Evaluation Plot

The correlator evaluation plots shown in Figures 96 and 101 through 103 show the effect of the sequence length 512, 256, 128, and 64 on the correlation output. The plots show that the signal-to-noise ratio is much lower at a sequence length of 64 than at 512.

The correlator evaluation plots shown in Figures 104 through 106 show the effect of the transmit/sample frequencies, 15 MHz, 30 MHz, and 60 MHz, on the correlated output. A 5 MHz transducer was used to prevent aliasing at the lower transmit/sample frequencies.

The correlator signal detection evaluation plots are shown in Figures 107 and 108. For this evaluation, the signal return from the transducer was attenuated at the input to the amplifier. The amplifier gain was increased to insure adequate noise interference on the signal return. Figure 107 shows the plot of the waveform produced at the output of the standard pulser/receiver. Figure 108 shows the plot of the waveform produced at the output of the correlator.

The flaw detection evaluation was conducted with an immersion type transducer aligned on the #1 Flat Bottom Hole, #7075-1-300 test block. Figures 109 through 111 show the results of the evaluation. The plots show the flaw return with the back surface return for the transmit/sample frequencies of 15 MHz, 30 MHz, and 60 MHz and the sequence lengths of 128, 256, and 448, respectively. The sequence length was selected for the particular transmit/sample frequency to insure that the uncorrelated flaw return would not interfere with the back surface return. It has been observed that the signal-to-noise ratio of the correlated output will decrease significantly when the return signals overlap. This condition remains to be explained.

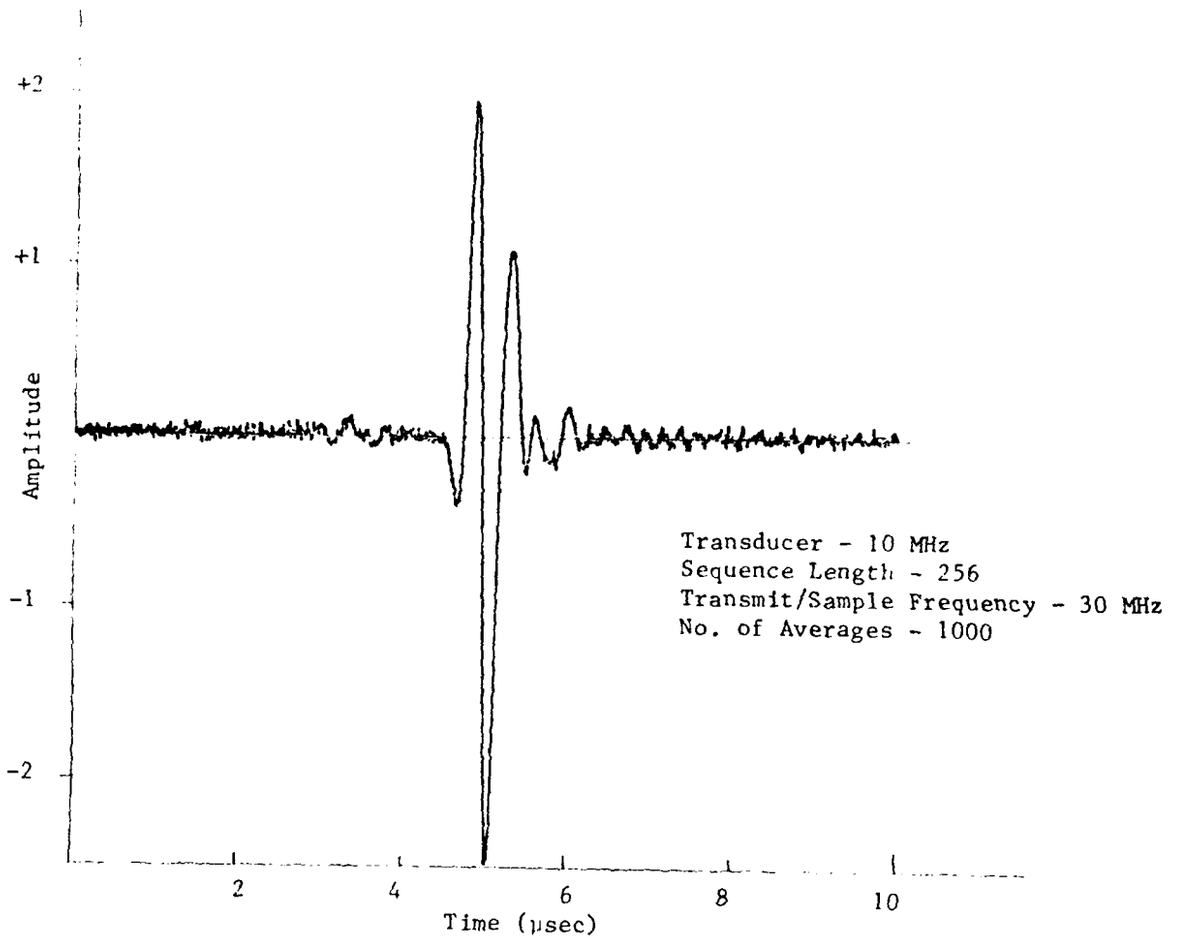


Figure 101. Correlator Sequence Length Evaluation Plot

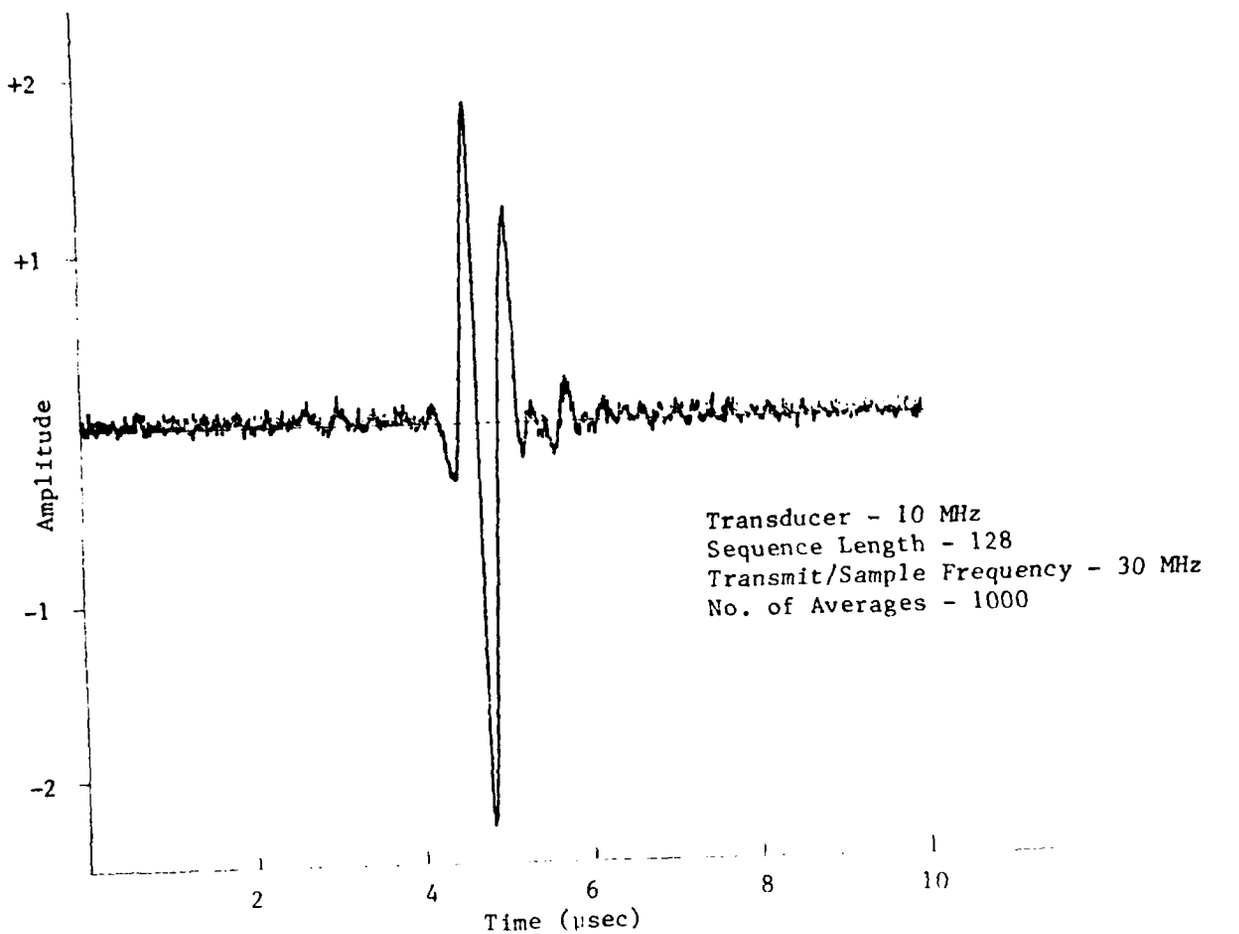


Figure 102. [illegible]tor Sequence Length Evaluation Plot

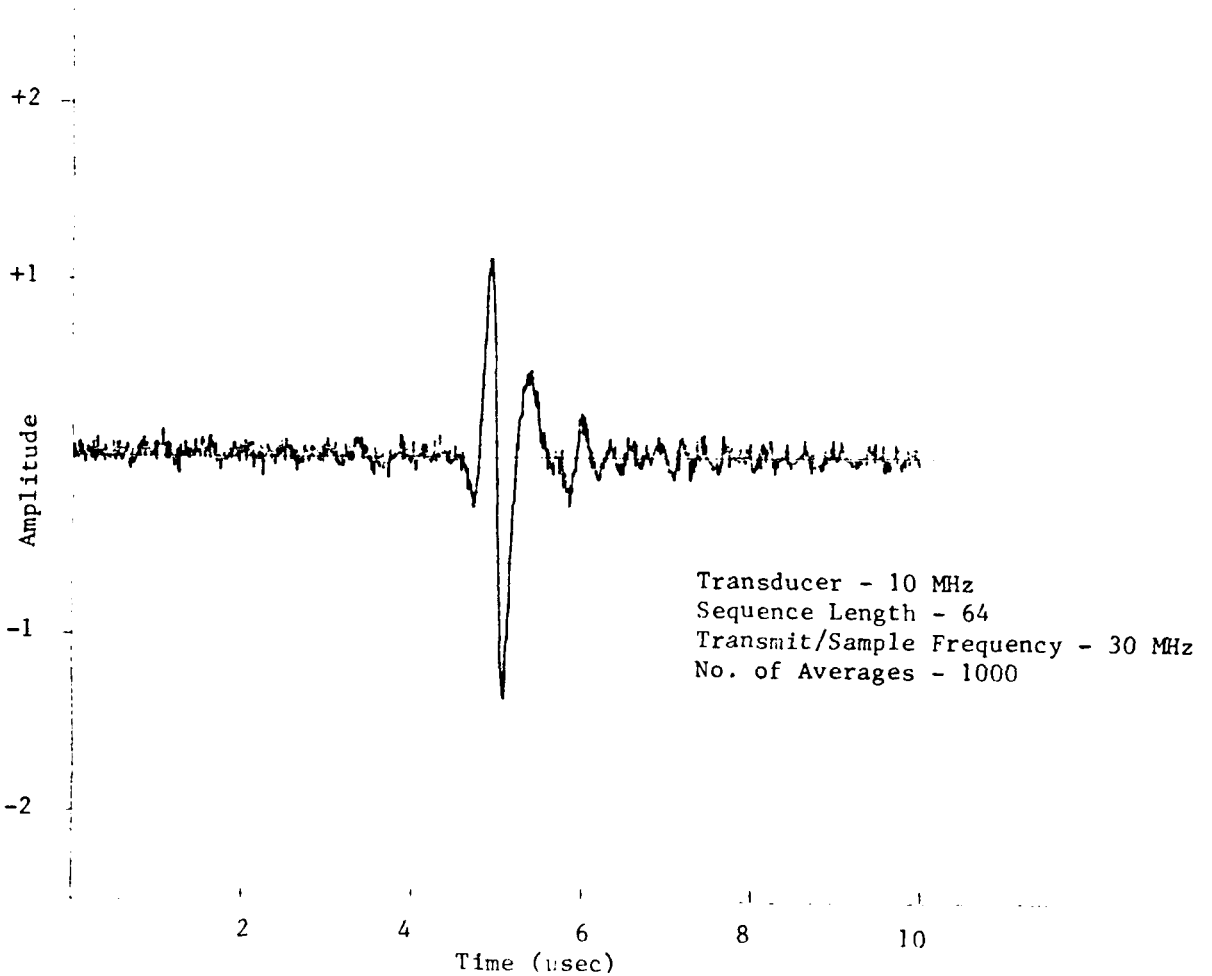


Figure 103. Correlator Sequence Length Evaluation Plot

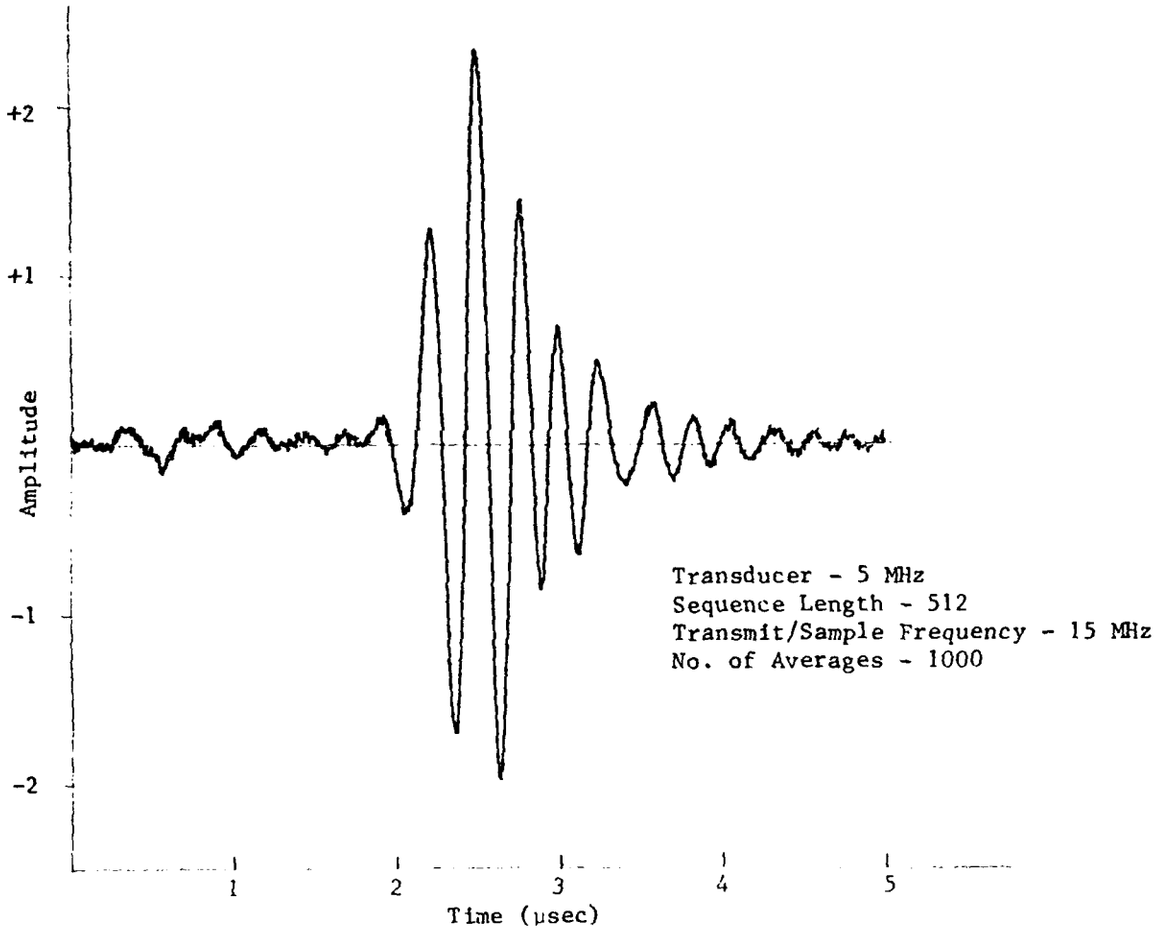


Figure 104. Correlator Transmit/Sample Evaluation Plot

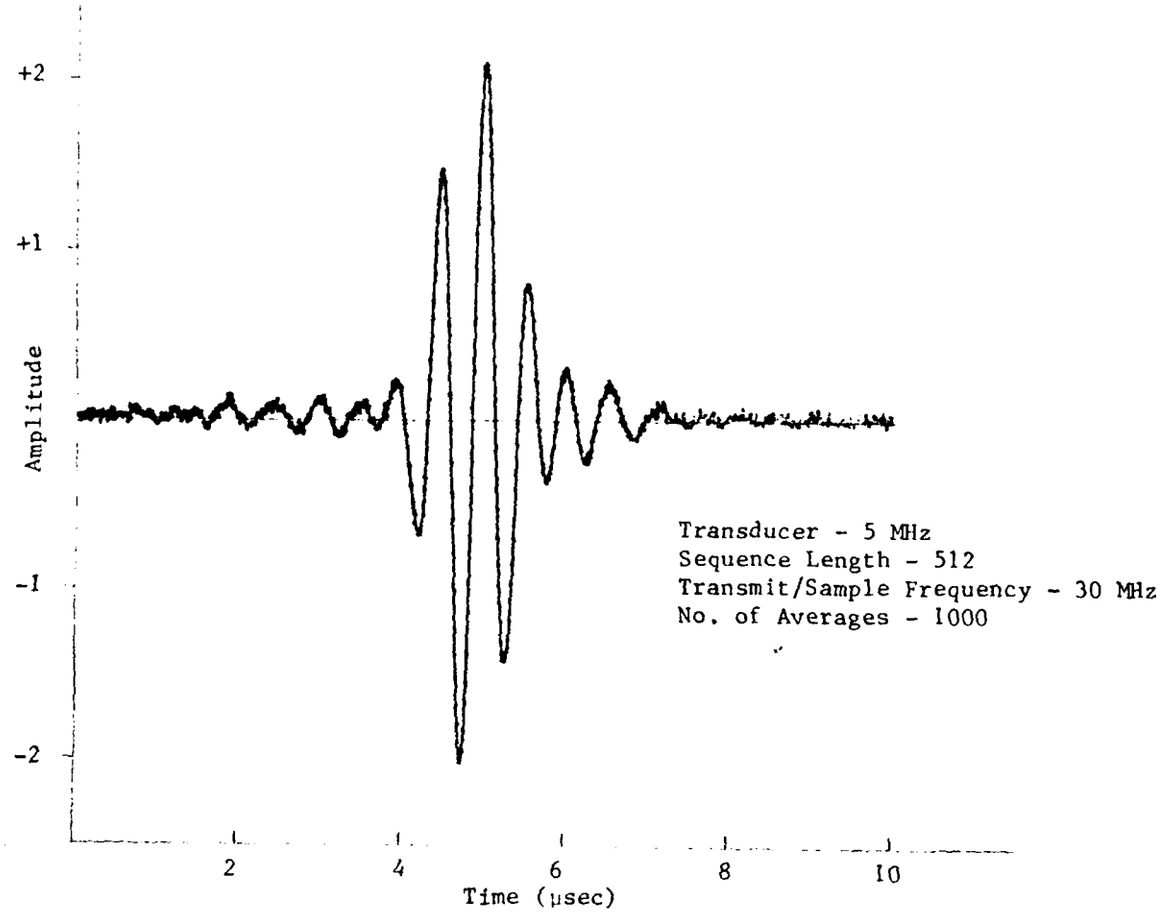


Figure 105. Correlator Transmit/Sample Evaluation Plot

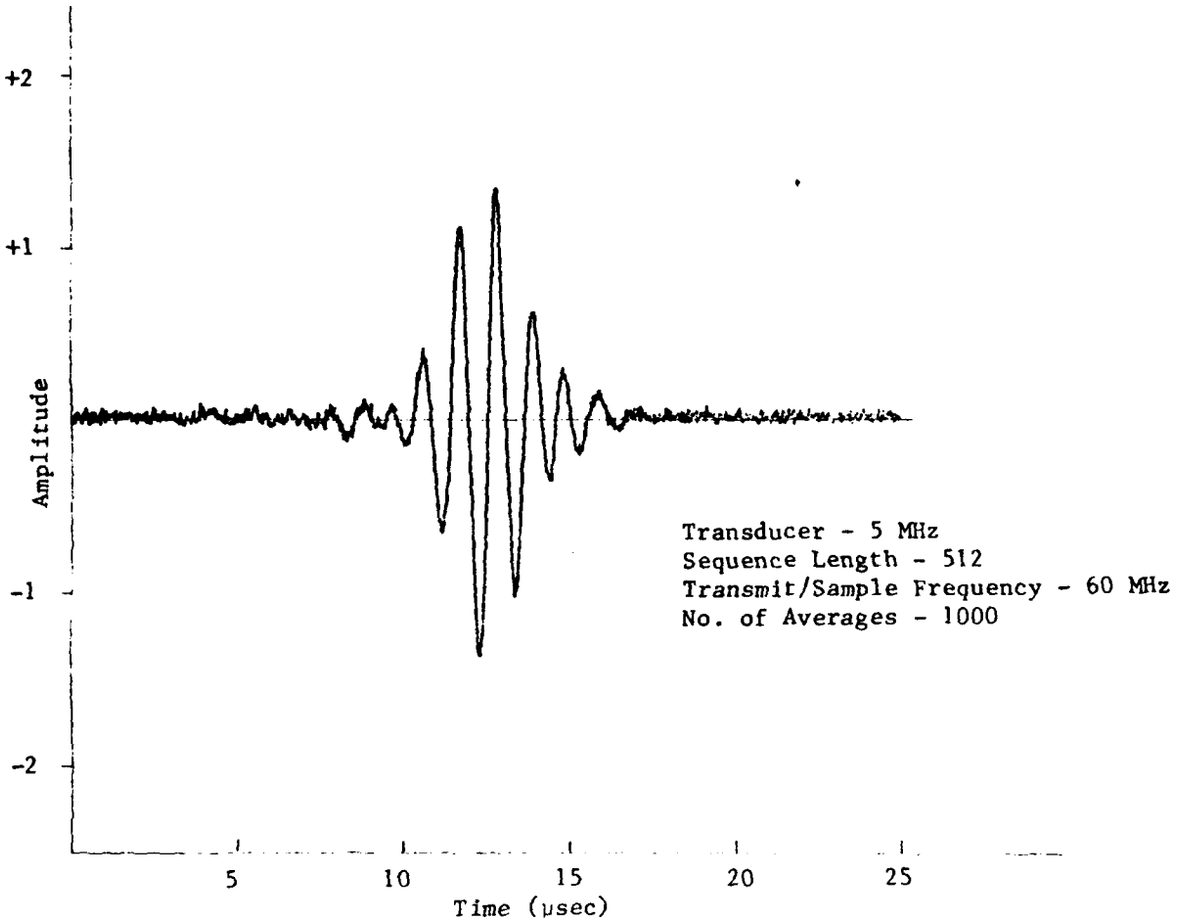


Figure 106. Correlator Transmit/Sample Evaluation Plot

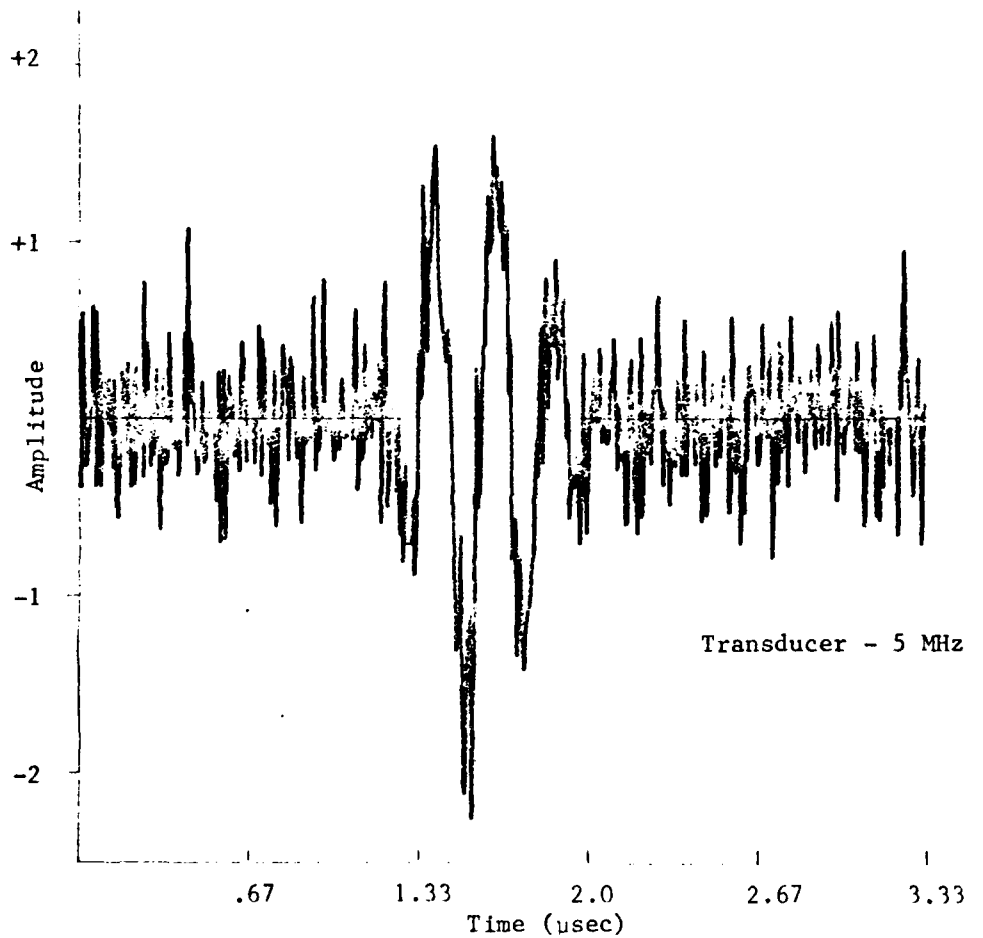


Figure 107. Pulser/Receiver High Noise Signal

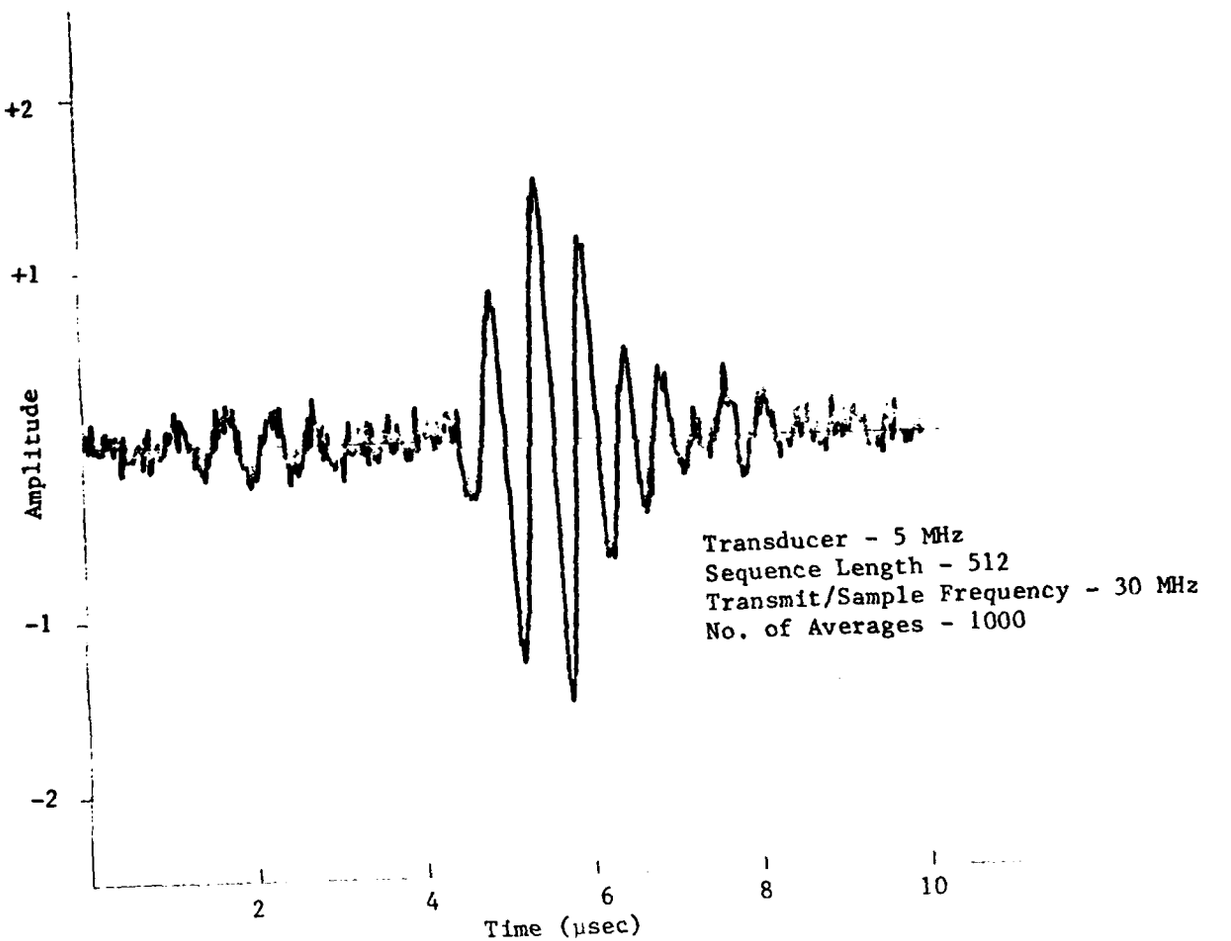


Figure 108. Correlator Signal Detection Evaluation Plot

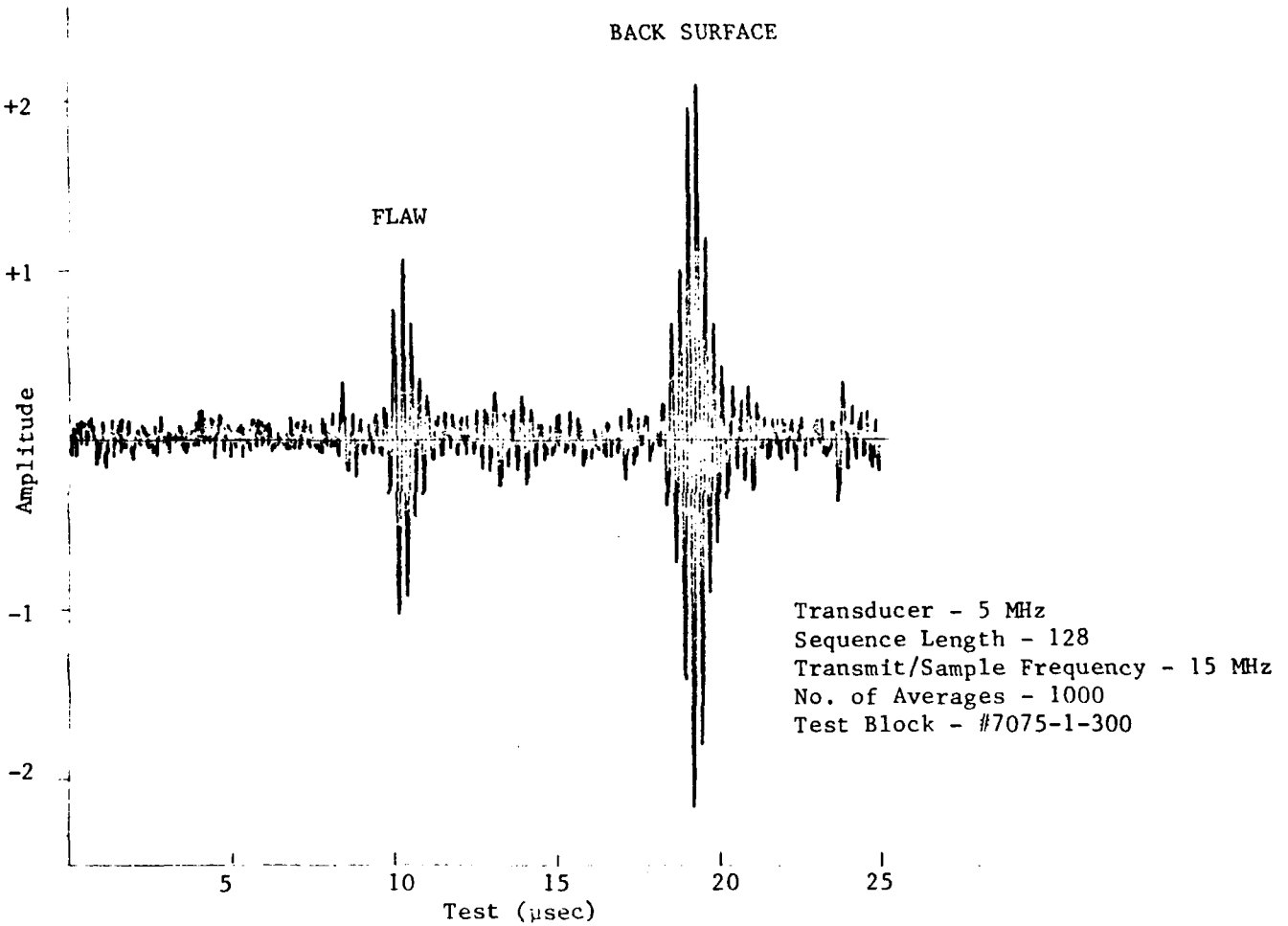


Figure 109. Correlator Flaw Detection Evaluation Plot

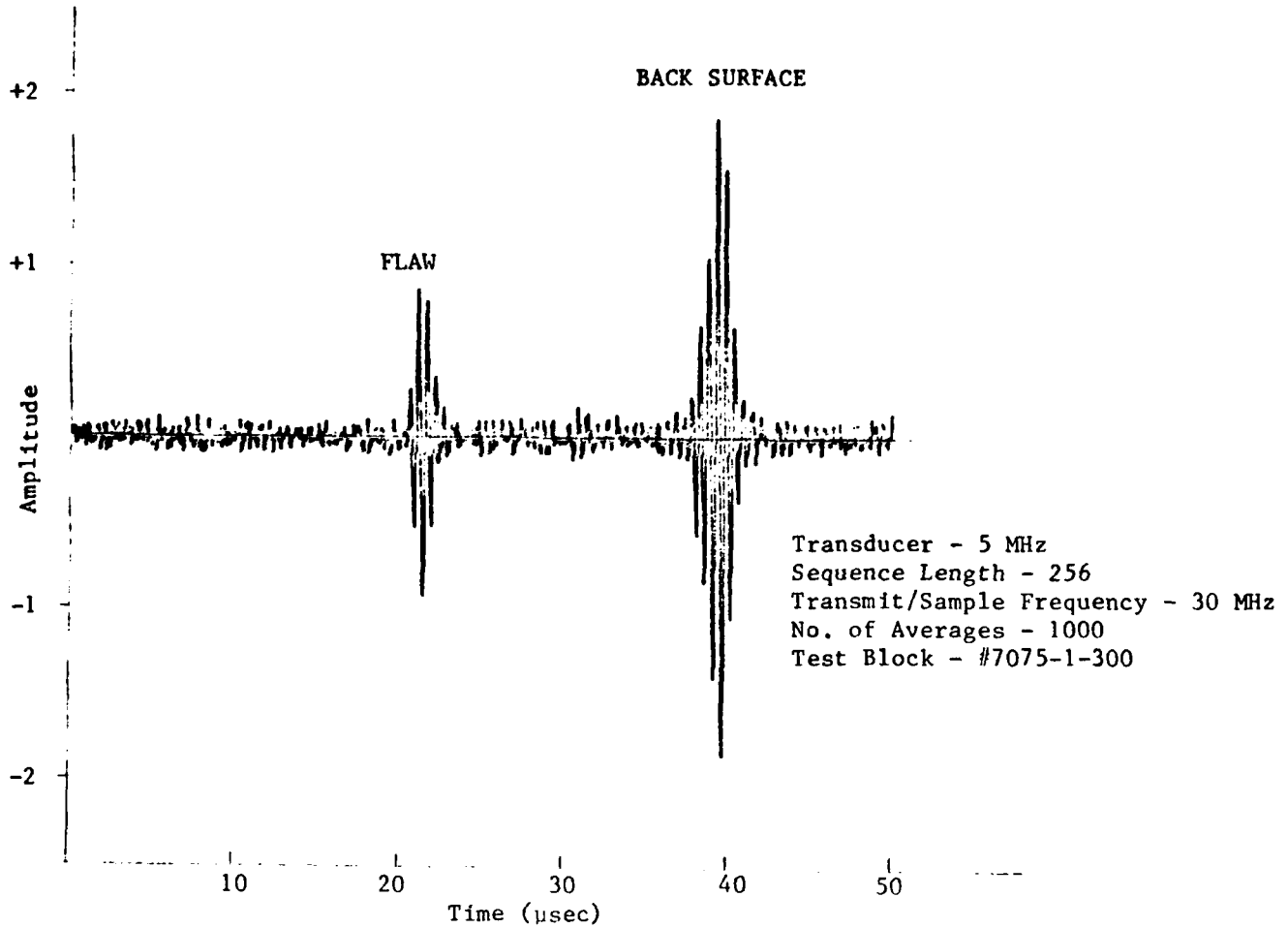


Figure 110. Correlator Flaw Detection Evaluation Plot

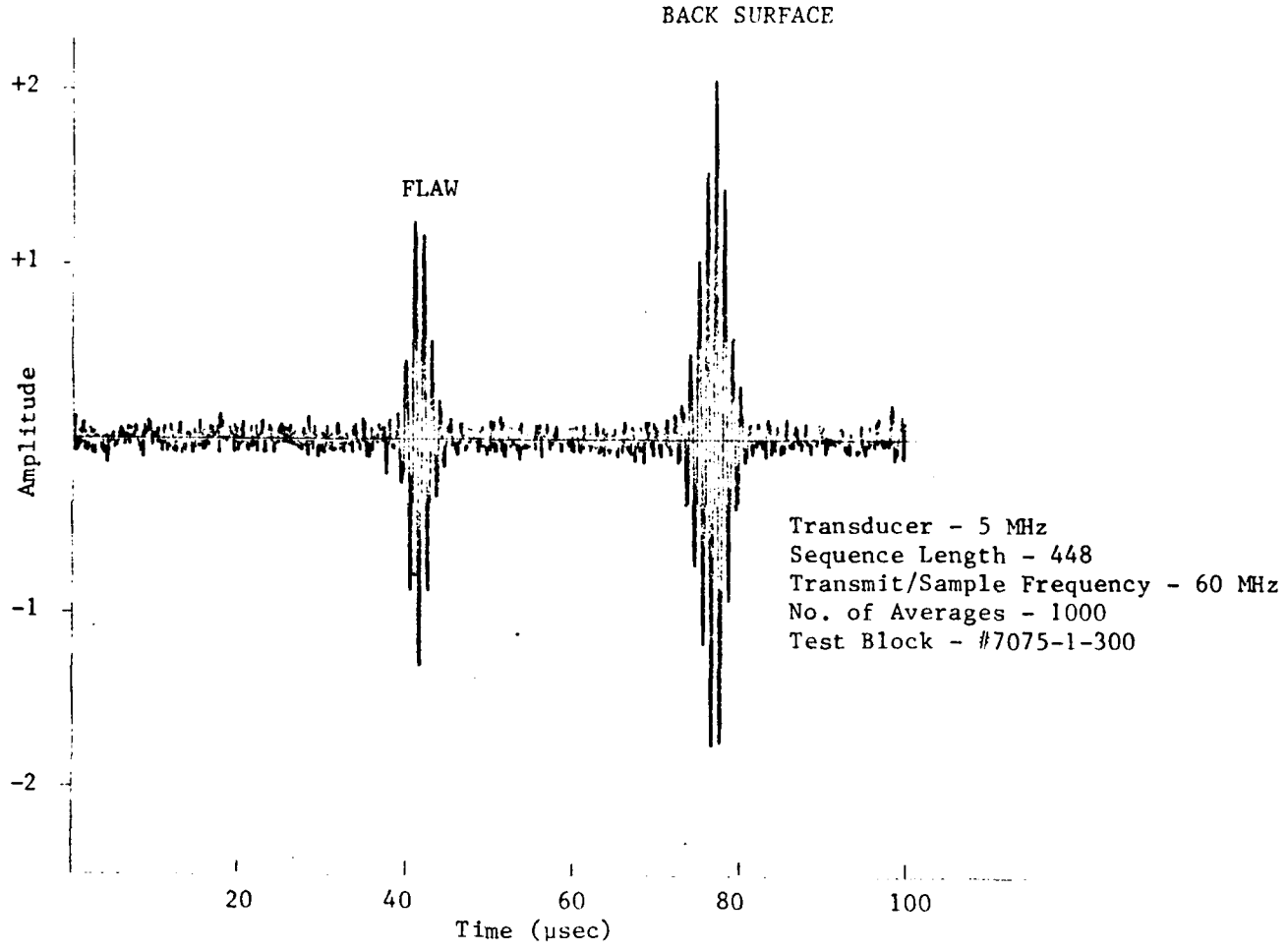


Figure 111. Correlator Flaw Detection Evaluation Plot

## 18. SUMMARY

The overall goal of this program was to develop a digital ultrasonic correlation system for NDE application of greater versatility and capability than the successful analog system developed in-house at AFWAL/MLLP. SRL had only limited success in meeting this overall goal. The program broke into two complementary tasks: (1) development of an all-digital Pulser/Receiver with a bandwidth of 85 MHz and a maximum gain of 80 dB; and (2) development of a pseudo-random correlation unit. The Pulser/Receiver met all of its necessary requirements; however, the correlation unit suffered from a technical design decision made early in the program as to the number of "bits" used in the correlation process. The decision (based upon both cost and the results of the computer model of an 8-bit correlation system) was to utilize 1-bit correlation. This choice led to an unavoidable (and most undesirable) nonlinearity in the correlated signal output when the input signal/noise ratio approached unity. This unfortunate consequence has restricted the versatility and capability of the entire system.

In its favor, the system has demonstrated the basic principle of an all-digital approach to pseudo-random signal correlation. Also, the computer model indicated that the possibility exists for compensating for the nonlinearity in the microcomputer. The current hardware system will allow this approach to be further pursued after a more exhaustive laboratory evaluation provides the necessary corrective algorithms.

In conclusion, SRL believes that the equipment it has delivered can prove quite useful to the United States Air Force in confirming the eventual practicality of a digital pseudo-random correlation system. It is recommended that further effort be made to resolve the remaining technical problems uncovered through the course of this project.

# APPENDIX A

# SYSTEM PRELIMINARY HAZARD LIST

## FOREWORD

This System Preliminary Hazard List (PHL) has been prepared in accordance with United States Materials Laboratory, Air Force Wright Aeronautical Laboratories (AFWAL), Contract No. F33615-79-C-5020, dated 29 May 1979. The analysis fulfills the requirements of the Contract Data Requirements List (CDRL), Sequence No. 8, and applicable portions of MIL-STD-882 and DI-H-3278/M.

## INTRODUCTION

The Advanced Nondestructive Evaluation (Ultrasonic Pulser/Receiver Technology) (henceforth referred to as the Pulser/Receiver and Correlator) safety requirements, as defined in the CDRL, include development of a PHL. The primary objectives of the PHL are:

1. To define the safety interfaces between the Pulser/Receiver and Correlator, the input power, and the operator/maintenance personnel.

2. To verify compliance with safety criteria.

3. To identify possible independent, dependent, and simultaneous failures which could represent a hazardous condition.

## ELECTRICAL POWER

The Pulser/Receiver and Correlator are electronic instruments which operate on 117 volt ac line power. The power input is by a three-way grounded plug. The 117 volts enter a fused, shielded line filter and is then distributed to the input transformers of the

modular system supplies. The only high voltages are generated by the pulser supply, within the Pulser/Receiver. The output of the pulser supply will vary from approximately 100 to 1200 volts dc, depending on the pulser volts switch setting (located on the front panel). This supply is enclosed in a grounded metal case.

The output of the pulser supply is connected to the input of the pulser supply switch through an insulated high voltage wire. A silicon rubber cement coating was applied to the solder connection at the input to the pulser supply switch. The output of the pulser supply switch will be equal in amplitude to its input but with only 25 microseconds pulse duration. The output average power will depend on the pulser volts and PRF switch settings. This circuit is enclosed in a grounded metal case.

The output of the pulser supply switch is connected to the pulser switch through coax cable. The output of the pulser switch is used to drive the ultrasonic transducer with a pulse amplitude approximately equal to its input. The pulse duration will not exceed more than 5 microseconds which yields very low average power. The pulser switch is enclosed in a grounded metal case.

HAZARD CATEGORY

The hazard categories of MIL-STD-882 were used: (Note: MIL-STD-882 categories are used as required by the contract rather than MIL-STD-882A which reverses the categories.)

Category I - Negligible
Category II - Marginal
Category III - Critical
Category IV - Catastrophic

The quantitative probability estimates of USAF DI-H-3278 were used: (Note: DI-H-7048 replaces DI-H-3278, but DI-H-3278 is used as required by the contract.)

| | Level | Specific Individual Item |
|---|---|---|
| Frequent | 6 | Likely to occur frequently |
| Reasonably Probable | 5 | Will occur several times in life of individual item |
| Occasional | 4 | Unlikely to occur in life of one specific item |
| Remote | 3 | So improbable that it can be assumed that this item will not be experienced |
| Extremely Improbable | 2 | Probability of occurrence cannot be distinguished from zero |
| Impossible | 1 | Physically impossible to occur |

INTERFACES

The following PHL defines the hazards between the Pulser/ Receiver, the Correlator, the input power, and the operator/ maintenance personnel.

PRELIMINARY HAZARD LIST

| Reference No. | Component or Item | Phase of Operation | Malfunction Condition | Results of Malfunction Condition | Potential Hazard | Hazard Category | Hazard Probability |
|---|---|---|---|---|---|---|---|
| 1 | Pulser/Receiver | Transducer hookup to coaxial cable | Coaxial cable connected to transmitter output | Pulse on transducer shield | Operator receives electrical shock | I | 5 |
| 2 | Pulser/Receiver | Coaxial cable hookup | Operator installs coaxial cable in wrong connector | Improper operation | Damage to equipment | II | 3 |
| 3 | Pulser/Receiver | Maintenance | Power switch inadvertently left on | Electrical power applied to Pulser/Receiver | Maintenance personnel receives shock | II | 3 |
| 4 | Pulser/Receiver | Maintenance/operation | Moving unit | Lift of unit by one man | Possible operator/ maintenance personnel back injury | I | 3 |
| 5 | Correlator | Coaxial cable hookup | Operator installs coaxial cable in wrong connector | Improper operation | Damage to equipment | II | 3 |
| 6 | Correlator | Maintenance | Power switch inadvertently left on | Electrical power applied to Correlator | Maintenance personnel receives shock | II | 3 |
| 7 | Correlator | Maintenance/operation | Moving unit | Lift of unit by one man | Possible operator/ maintenace personnel back injury | I | 3 |

APPENDIX B

SYSTEM PARTS LIST

The following is a parts list for the Pulser/Receiver and Correlator.

Integrated Circuits

SN7404 - Texas Instruments
SN7406 - Texas Instruments
SN7407 - Texas Instruments
SN7412 - Texas Instruments
SN7475 - Texas Instruments
SN74123 - Texas Instruments
SN74138 - Texas Instruments
SN74154 - Texas Instruments
SN74191 - Texas Instruments
SN75451 - Texas Instruments
SN74LS02 - Texas Instruments
SN74LS04 - Texas Instruments
SN74LS08 - Texas Instruments
SN74LS21 - Texas Instruments
SN74LS32 - Texas Instruments
SN74LS74 - Texas Instruments
SN74LS75 - Texas Instruments
SN74LS123 - Texas Instruments
SN74LS125 - Texas Instruments
SN74LS126 - Texas Instruments
74F00 - Fairchild
74F04 - Fairchild
74F10 - Fairchild
74F32 - Fairchild
74F74 - Fairchild
74L5154 - Fairchild
DM8551N - National
TDC1004J - TRW
TDC1007PCB - TRW
SN74LS173 - Texas Instruments
SN74LS197 - Texas Instruments
SN74LS221 - Texas Instruments
SN74LS240 - Texas Instruments
SN74LS241 - Texas Instruments
SN74LS365 - Texas Instruments
SN74LS367 - Texas Instruments
SN74LS368 - Texas Instruments
SN74LS373 - Texas Instruments
SN74LS374 - Texas Instruments
SN74500 - Texas Instruments
SN74504 - Texas Instruments
SN74511 - Texas Instruments
SN74586 - Texas Instruments
SN745112 - Texas Instruments
SN745140 - Texas Instruments
SN745195 - Texas Instruments
SN745240 - Texas Instruments
95016 - Fairchild
95231 - Fairchild
10125 - Fairchild
10474 - Fairchild
93425A - Fairchild
8085A - Intel
8282 - Intel
8286 - Intel
8291 - Intel
ICM7226A - Intersil

## Linear Circuits

ADOP-07 - Analog Device
AD571 - Analog Device
AD7524 - Analog Device
THS-0025 - Analog Device
LF355 - Signetics
LFT355 - National Semiconductor
LH0002 - National Semiconductor
LH0002CN - National Semiconductor
LM117HVH - National Semiconductor
LM376N - National Semiconductor
MWA120 - Motorola
AM685DL - Advanced Micro Devices
DG501 - Siliconix
HA5195 - Harris
TIL-74 - Litronix
TL441 - Texas Instruments
UA733 - Fairchild
2N5114 - Intersil
3N211 - RCA Solid State
PSCJ2-2 - Mini Circuits Labs.
GA301 - Unitrode

## Relays

196TS1A2M-5S - Sigma, SPST
846A2 - Condo, SPST
J411-5 - Teledyne, SPDT
712TN - Teledyne, DPDT

## Transistors

MJ12004 - Motorola
MJ12005 - Motorola
MPSH10 - Motorola
MPSU60 - Motorola
MPSH81 - Motorola
2N3866 - Motorola
2N5583 - Motorola
J309 - Siliconix (FET)
VN10KM - Intersil
2N3904 - National
2N3906 - National

## Crystals

10 MHz Clock Oscillator Hy 4550 - Hytek
10 MHz - Intel
6 MHz - Intel


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